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Serial No.: 09/396,352 11/11/2002 DOCKET NO.: NOVA-002-C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Tümay TÜMER

Serial No.: 09/396,352

Art Unit: 2736 12-6-02

Filed: September 14, 1999

Examiner: HUANG, S

For: TAG HAVING A SEMICONDUCTOR CHIP AND METHOD OF ATTACHMENT TO ARTICLE

DECLARATION OF TÜMAY TÜMER

I, Tümay O. Tümer, hereby declare that:

(1) I am the Tümay O. Tümer who is the named inventor in the above captioned case and I submit this declaration under 37 CFR § 1.131.

(2) Attached hereto are documents which bear Bates Numbers 000001 - 000106. Bates Numbers 000001 - 000026 are a proposal for a practical system for low cost smart tag and an applicator submitted by NOVA R & D on July 5, 1996. Bates Numbers 000027 - 000056 are an award/contract given to NOVA R & D by the Department of the Army for services set forth in the proposal (Bates Numbers 000001 - 000026). Bates Numbers 000057 - 000106 are a proposal for a Phase II Small Business Innovation Research contract having a title of "Low Cost Practical MicroTAG and Tag Applicator System" which is dated August 6, 1997. Bates Number 000107 is a blown up clear photograph of Figure 9 shown at Bates Number 000071. In the initial proposal at Bates Number 000008, there is

shown at the bottom of the page with respect to discussion of the antenna circuit for the smart tag, the proposed use of a closed loop, and other antenna types, such as a dipole (see line 4 up from the bottom). The rest of the proposal (Bates Numbers 000001 - 000026 outlines the proposal for the construction of the silicon chip which would comprise the smart tag.

(3) At page 000045, the award of the contract states that it is for a feasibility study for developing a practical low cost smart tag using a radio frequency and microwave.

(4) In the Phase II proposal, it is stated at page 000059 that the phase 1 feasibility study of the smart tag chip had been completed. Still further, a prototype version of the tag was designed and fabricated. This device is shown at page 000071, and in a separate photograph which is numbered 000107. Page 000107 is a blown up, clear photograph of the tag sitting on a chip shown at Figure 9 at page 000071.

(5) At page 000064 there is a description of work done in the Phase I contract. This relates to the fabrication of the prototype (shown on the dime), and which would result in a successful simulation in design during Phase I. The chip is described as having two antennas. One to power

the chip and/or receive data and the other to transmit data.

(6) At page 000069, line 3 down from the top, Applicant notes that a dipole antenna can be driven between a half wave and quarter wave reflector. This conclusion is based upon fundamental engineering principles and was known at the time.

At page 000071 there is shown a photograph of the microTAG produced in the Phase I contract. Note: This photograph is also shown enlarged at page 000107.

At page 000073 there is shown a layout of the tag chip. In this layout the back scatter antenna (5) (which may be a dipole (see page 000069), receiving antenna 7, as the capacitor array for poser storage (6R) shown. Section 7 is the larger one and is a power receiving and data receiving antenna. The data transmitting antenna is the thinner one (antenna 5). The spiral antenna is not shown. The design was two dipole antenna in place of a spiral antenna. One or both power and data receiving (the think one 7) and a separate dipole antenna (the thin one 5). There were only dipole antennas on this chip.

(7) At page 000091 (the Phase II proposal) at the bottom, The antenna circuit is described for the Phase II chip. It is stated that the antenna will be designed to have a

maximum possible power from a remote programmer reader and store it on a capacitor. Here it should be noted that a programmer/reader was not constructed in Phase I and, therefore, such a test could not be made. Still further, in the current chip (chip built under Phase I), a "simple patch antenna was used". However, as stated at the top of page 000092, other antenna types, such a dipole, half wave, quarter wave, were to be studied.

(8) It was known that each type of antenna, such as patch, dipole, half wave, and quarter wave, had its own benefits and problems (see top of page 000092). However, there was no doubt that each type of antenna would work on a chip as proposed.

(9) During the period from August 6, 1997 (submission of the Phase II proposal) until the filing of the provisional application on September 14, 1998, Applicant was continuously seeking to obtain additional funding under the SBIR and other program proposals. This was in order to further Applicant's developments of its chip.

(10) The owner of this invention (Tümay O. Tümer) in 1997 and 1998 employed a total of 3 scientists and necessary support personnel. NOVA simply could not afford to sustain its research personnel without government support

during this time. Stated simply, NOVA did not have discretionary funds known as IR&D (Independent Research and Development) which are available only to large government contractors and, therefore, NOVA could not afford to carry forward research on its own.

(11) I further state that as the owner of this invention, and 100% owner of NOVA R & D, Inc., I also was not in a position financially to afford the sustained research without government support in the time between August 6, 1997 until September 14, 1998.

(12) I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

T. Tümer

Tümay O. Tümer

11/12/2002

Date

Attachments

Reference A
DoD SBIR Solicitation 96.2

TO: NOVA R&D, Inc.
Fill in firm's name and mailing address

SUBJECT: SBIR Solicitation No. 96.2
Topic No. A96-009
Fill in Topic No.

This is to notify you that your proposal in response to the subject solicitation and topic number has been received by

Army SBIR Office
Fill in name of organization to which you will send your proposal.

Signature by receiving organization

5 JUL 96
Date

See page 1. dipole antenna

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000001

U.S. DEPARTMENT OF DEFENSE

SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM
PROPOSAL COVER SHEET

Failure to fill in all appropriate spaces may cause your proposal to be disqualified

TOPIC NUMBER: A96-009

PROPOSAL TITLE: A Practical System For A Low Cost Smart Tag And Applicator

FIRM NAME: NOVA R&D, Inc.

MAIL ADDRESS: 1525 Third Street, Suite C

CITY: Riverside STATE: CA ZIP: 92507

PROPOSED COST: $99,938.00 PHASE I OR II: 1 PROPOSAL PROPOSED DURATION: 6 IN MONTHS

BUSINESS CERTIFICATION:

	YES	NO
▸ Are you a small business as described in paragraph 2.2?	☒	☐
▸ Are you a minority or small disadvantaged business as defined in paragraph 2.3? (Collected for statistical purposes only)	☐	☒
▸ Are you a woman-owned small business as described in paragraph 2.4? (Collected for statistical purposes only)	☒	☐
▸ Have you submitted proposals or received awards containing a significant amount of essentially equivalent work under other DoD or federal program solicitations? If yes, list the name(s) of the agency or DoD component, submission date, and Topic Number in the spaces below.	☐	☒

▸ Number of employees including all affiliates (average for preceding 12 months): 7

PROJECT MANAGER/PRINCIPAL INVESTIGATOR	CORPORATE OFFICIAL (BUSINESS)
NAME: Dr. Jianping Peng	NAME: Ms. Sezen H. Tumer
TITLE: Engineer	TITLE: President
TELEPHONE: (909) 781-7347	TELEPHONE: (909) 781-7332

For any purpose other than to evaluate the proposal, this data except Appendix A and B shall not be disclosed outside the Government and shall not be duplicated, used or disclosed in whole or in part, provided that if a contract is awarded to this proposer as a result of or in connection with the submission of this data, the Government shall have the right to duplicate, use or disclose the data to the extent provided in the funding agreement. This restriction does not limit the Government's right to use information contained in the data if it is obtained from another source without restriction. The data subject to this restriction is contained on the pages of the proposal listed on the line below.

PROPRIETARY INFORMATION: 3 to 25

000002

SIGNATURE OF PRINCIPAL INVESTIGATOR	DATE	SIGNATURE OF CORPORATE BUSINESS OFFICIAL	DATE
	7/3/96		7/3/96

U.S. DEPARTMENT OF DEFENSE

SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM

PROPOSAL COVER SHEET

Failure to fill in all apropriate spaces may cause your proposal to be disqualified

TOPIC NUMBER: A96-009

PROPOSAL TITLE: A Practical System for a Low Cost Smart Tag and Applicator

FIRM NAME: NOVA R&D, Inc.

PHASE I or II PROPOSAL: 1

Technical Abstract (Limit your abstract to 200 words with no classified or proprietary information data.)

A feasibility study is proposed for developing a practical low cost smart tag and a remote programmer/reader system using a radio frequency link. The required information will be stored in the tag's non-volitile memory. The information can be written and read out as many times as needed.

A novel applicator for the smart tag is also proposed. The applicator will be simple in design. It will apply the smart tag onto any type of package, box, bag, luggage, and crate of various thickness and stiffness while they are transported on a conveyer. The tag will be applied to the item as it is moving with arbitrary order, shape, size, orientation, and position. The conveyor can reach maximum speed of two hundred feet per minute. The material covering the item can be cloth, metal, plastic, paper or wood.

During Phase I, the feasibility of the smart tag and the applicator will be experimentally demonstrated. During Phase II, prototypes of the smart tag, the remote programmer/reader system and the versatile applicator will be fabricated. In Phase III, smart tag, remote programmer/reader system and the tag applicator will be commercialized.

Anticipated Benefits Potential Commercial Applications of the Research or Development.

The results of the Phase I and II programs will be a practical low cost smart tag, a remot programmer/reader system and a novel versatile applicator. The smart tags and the applicator can be used for tagging any type of conveyor transported item. It can also be used in many other applications where automatic tagging is required.

List a maximum of 8 Key Words that describe the Project.

Tags	Smart Tags
Remotely programmable tags	Tag applicator
	000003

Number of this page if classified or proprietary information data

Proposal page No. 1

A. IDENTIFICATION AND SIGNIFICANCE OF THE PROBLEM

A. 1. Problem

Smart tags are presently used for a number of applications in both the civilian and military sectors. These applications include item identification, toll passes and barrier tagging. These tags are relatively expensive, cost several dollars and are limited in the amount of information they can store. These tags cannot be used in large quantities, because of the cost involved, especially in circumstances where they can not be recovered for reapplication.

Both military and civilian sectors require low cost tags costing less than 50 cents each for many different applications especially for use in large quantities where tag recovery is impractical. Some applications for Government use include tagging individual weapons, munitions or pieces of equipment, crates and other inventory. Some civilian applications include tagging baggage in airports, parcels, packages, crates, individual items, files, folders and dockets, inventory, shop merchandise, and for employee and vehicle identification.

Tagging baggage at airports is an important application. It will be beneficial to have a smart baggage tagging system which can store detailed information. This will allow to track the history of baggage: point of origin, travel route, and a profile of the owner. Such information will require significant amount of non volatile memory.

The size of the tag is also important so that it can be placed onto baggage and cargo inconspicuously. Therefore, the size of the tag should be smaller than about 5 mm^3.

The tag should not require any external power. Even tiny batteries will increase the size and complexity due to the connection of the battery to the chip, at the same time tag's cost increases dramatically. A battery has a finite lifetime and the probability of failure during application is greater. A tag with the required power generated onboard by the remote programmer/reader would be a better solution for accommodating power needs

Development of such a smart tag requires a suitable applicator. The applicator must be simple in design and cost effective. The applicator must be able to apply the smart tag onto any type of package, bag, box, luggage, and crate of various thickness and stiffness while they are transported on a conveyer. The applicator must apply the tag onto the baggage item as it is moving with arbitrary order, shape, size, orientation and position. It must work fast as the conveyer can reach a maximum speed of two hundred feet per minute with about 3 feet spacing between each item. The tag must adhere easily to different kinds of luggage material such as, cloth, metal, plastic, paper, leather or wood.

A Phase I program is proposed to study the feasibility of a practical low cost smart tag, a remote programmer/reader system and a novel applicator that can solve and meet the requirements stated above.

A. 2. Proposed Smart Tag Concept

A practical tag built on a tiny silicon chip is proposed here. The size of the chip will be between 1 x 1 x 0.3 mm to 3 x 3 x 0.3 mm. The chip will be completely self contained. The final chip will have no connections pads. However, the initial prototypes may have pads for testing and debugging. It will have an antenna placed around the circumference of the chip. The process to be used for the final product is expected to be 0.35 to 0.8 micron, although the Phase I and Phase II prototypes may be manufactured with 1.2 micron process.

The length of the antenna can be fairly long, if proper attention is paid to the wave nature of the electric fields on the silicon substrate. A computer aided design (CAD) program developed for modeling three dimensional silicon layout structures will be used to design and simulate the antenna. In this work the spacing and thickness of the antenna metal will be optimized for application to the proposed smart tag chip. For example, at 10 GHz the microwave skin depth is 0.8 micrometers to

achieve low resistivity. The skin depth is the distance the microwave currents penetrate into the surface of the metal layer. It is within this characteristic depth that the electromagnetic field propagates. This skin depth varies with the frequency and dielectric constant of the surrounding media. Careful attention will be paid during modeling and simulations, to the wave nature of the interaction to achieve optimum design. (Very short radio waves or microwaves will be used for this project to achieve higher efficiency.)

The external remote programmer/reader will send out radio frequency power to the antenna on the chip. The received power will be used to charge up a capacitor. The output of the capacitor will then be used to power the chip. The rest of the circuit on the chip will be low power CMOS circuits that will receive the signal from the remote programmer/reader and store the information onto the non volatile EEPROM memory. If a read request comes from the programmer/reader the chip will also have the functionality to transmit the contents of the memory through the antenna.

Other functions such as having a unique tag number for identification of which tag is programmed or read out will also be studied and implemented if required. Such a unique identification number can be important if there is more than one tag inside the aperture field of the remote programmer/reader.

The cost of the chip will be kept as low as possible by using small die size on large 6" or 8" wafers. For example, from a single 8" wafer we expect to get approximately 30,000 1 x 1 mm, 10,000 2 x 2 mm and 3,000 3 x 3 mm dies. Small dies with relatively simple circuitry may have exceptionally high yield reaching up to 80%. In large quantities each wafer is expected to cost much less than $400 to process. This shows that even with 50% yield at $400 per wafer the fabrication cost of the tags is in cents. The cost of initial prototypes will be much higher due to the low numbers required and the large non-recurring engineering cost which includes the mask set.

A second factor involved in the cost is the selection of the working tags for deployment. Since the production tags will be completely self contained the testing will not require a probe card and a costly probe station. The dies can pass in front of a test and selection system placed on to a tiny conveyer belt. The test system will be very similar in design to the remote programmer/reader unit. It will be programmed to power the tag, write and read several coded data to test and select the working chips. It may also program a unique ID number on to the tag if required. Such a system can be built at NOVA during Phase III.

In summary, the remote programmer/reader will produce radio waves tuned to the tag antenna for transferring power to the chip. It will also transmit the data to the tag with or without an identification number. The identification number can be already programmed into the tag before application. It will also have the capability to ask the chip to send its memory contents and be able to read the data transmitted by the tag. Each cycle; send power, program tag, request data from tag and read tag, will be done sequentially. These and other possible functionality and circuit ideas will be studied during Phase I.

A. 3. Proposed Applicator Concept

The requirements for the applicator is extensive as described in **Section A1**. It is proposed a simple but novel technique to meet these requirements. The proposed applicator will be made of a simple glue gun. A jelly type of glue that does not harden but retains its stick quality for a long period of time measured in days will be used. The tags will be embedded into the glue and glue balls containing a tag will be propelled onto a baggage. The diameter of the glue ball will be between 3 to 5 mm. The glue will be the kind used for temporary attachment of paper, wood, plastic, metal or any kind of material to each other. Only problematic surfaces may be oily surface and possibly teflon. This type of glue practically attaches itself to any known material. The most effective glue will be selected during Phase I.

The selected glue can be transparent or may be used in different colors. A transparent glue can match most surfaces and will be the low cost way to proceed. However, it will show the silicon tag inside. If a colored glue is needed to match the color of the item then a color reader will be required such as a simple video camera. The output of the color video camera will be used to select the most appropriate glue color. This will also require several applicators or one applicator with several

nozzles one for each color. This will be studied during Phase I and implemented during Phase II.

The glue gun can be powered by several different techniques. One of the simplest could be the pressurized air. We will try to find an off-the-shelf glue gun during Phase I. This is expected to be the most cost effective approach. The glue gun may need some modification to be usable with the type of glue selected and for embedding the tag.

Pointing the glue gun may also be required if there will be small size items on the conveyer belt. This process will require the determination of the position of the item on the conveyer belt. The work on determining the position of the item on the conveyer belt and pointing gun to the right location will be investigated for feasibility during Phase I, studied during Phase II and implemented during Phase III if required.

A. 4. The Proposed Phase I Feasibility Study

The proposed Phase I feasibility study will be carried out both theoretically and experimentally. The proposed circuits will be carefully studied, enhanced, modeled, simulated and optimized. The main difficulty will be designing a circuitry for transferring and storing sufficient charge onto the tag chip. The second difficulty will be to transmit data back to the remote reader with sufficient power so that it could be received with high reliability. The rest of the circuit is expected to be challenging for low power implementation but not a major problem.

Some circuitry may be built using discrete components for some of the tests in the lab. Prototypes of the circuits modeled and developed will be layout on silicon and a prototype chip of about 2 x 2 mm size will be manufactured through the MOSIS program run by the University of Southern California. Test pads will placed at key sections of the prototype tag chip so that its functionality and performance can be tested using probes. Due to time and funding limitations it is expected that only one prototype chip can be manufactured during Phase I. However, the results obtained from this chip will help demonstrate its potential and save significant time and effort during Phase II.

The remote programmer/reader will be also studied during Phase I. The work will be mostly theoretical as the main focus and effort will be concentrated on the tag electronics. Some desk top work will be done such as transmitting power onto the tag and measuring the charge stored on the chip. Since there are no foreseen problems with the remote programmer/reader the work is more straight forward once a working tag chip is developed. Therefore, the remote programmer/reader will be fully designed and developed during Phase II.

A significant amount of work will be carried out on the tag applicator. The work will first focus on searching for the best glue for applying the tags onto baggage and cargo. Samples of glue will be purchased and tried on different kinds of baggage case materials for adhesion and nondestructive removal. Then the search will concentrate on a suitable glue gun. If a suitable candidate is found that will cost within funding available it will be bought and tried. Modification of the glue gun will be carried out if necessary. Whether there is a need to point the glue gun will be investigated.

A. 5. Phase II Objectives

During Phase II the design of the tag will be improved and optimized using the Phase I results. A second prototype will be manufactured. According to the results of the second prototype the final tag electronic circuit will be designed and sufficient number of tags will be manufactured for delivery to DoD/Army.

A prototype remote programmer/reader will be also designed and developed using the Phase I investigation results. The prototype manufactured will be delivered to DoD/Army together with the tags.

The applicator system will be also finalized during Phase II using the results obtained in Phase I. A prototype applicator will be developed during Phase II. The applicator will be also delivered to DoD/Army at the end of Phase II.

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B. PHASE I TECHNICAL OBJECTIVES

B. 1. Phase I Tasks

The tasks of proposed Phase I program are given below:

Task 1. Design and simulate the electronic circuits for the proposed smart tag system.

Task 2. Selectively layout the tag circuitry onto silicon with buffered pads at critical locations for testing and evaluating the circuits developed.

Task 3. Investigate different types of glues for use by the proposed tag applicator.

Task 4. Study performance of the selected glues on different baggage and cargo materials.

Task 5. Set up a test system for the prototype tag chips.

Task 6. Fabricate, test and evaluate prototype tag chips.

Task 7. Search for a suitable glue gun, evaluate possible candidates, study the modification of selected devices or if necessary design a custom glue gun.

Task 8. Investigate and prepare a preliminary design of a remote programmer/reader system for the tags.

Task 9. Study the charge transmission and storage on the tag chip.

Task 10. Investigate the capability of the tag circuitry to transmit data back to the remote reader.

Task 11. Present and demonstrate the Phase I results to DOD/Army officials.

Task 12. Write Phase I Final Report.

B. 2. Phase I Task Schedule

Work will start immediately on the design, modeling and simulation of the smart tag electronic circuits especially the antenna system (Task 1). This work is expected to take about 1 month. As soon as the simulations are completed the silicon layout of a prototype chip will begin (Task 2). This will take about 1.5 months to complete.

The investigation of the glue types will start as soon as the tag chip simulation is underway (Task 3). It will take about 1.5 months to complete the initial work. However, search for the best glue will carry on at a much reduced activity level until Phase III in case better products come to market. The performance of the selected glues will be studied (Task 4) for about one month.

A benchtop test system will be designed and developed (Task 5) as soon as the tag electronics is decided. This work is expected to take about 2 months. When the tag chip silicon layout work is completed it will be sent to manufacture using the low cost MOSIS program (Task 6). It will take about 6 weeks to fabricate the prototypes at the foundry. As soon as the chips arrive they will be tested and evaluated (Task 6). The total work is expected to take about 2 months.

A search will be carried out, as soon as a glue is selected, for a suitable glue gun (Task 7). If found the gun may be modified for tag application. If none can be found then a custom glue gun will be designed. This work is expected to take about 3.5 months.

As soon as the tag circuitry is decided the design of the remote programmer/reader will start (Task 8). It is expected to take about 3.5 months to complete. The charge (Task 9) and data transmission (Task 10) to and from the tag chip will be studied as soon as the tag chip testing is completed. These tasks will take about 1.5 months. The prototype tags and the work on the applicator will be presented to DoD/Army officials at the end of the project period (Task 11). The Phase I Final Report will be written during the final month of the project (Task 12).

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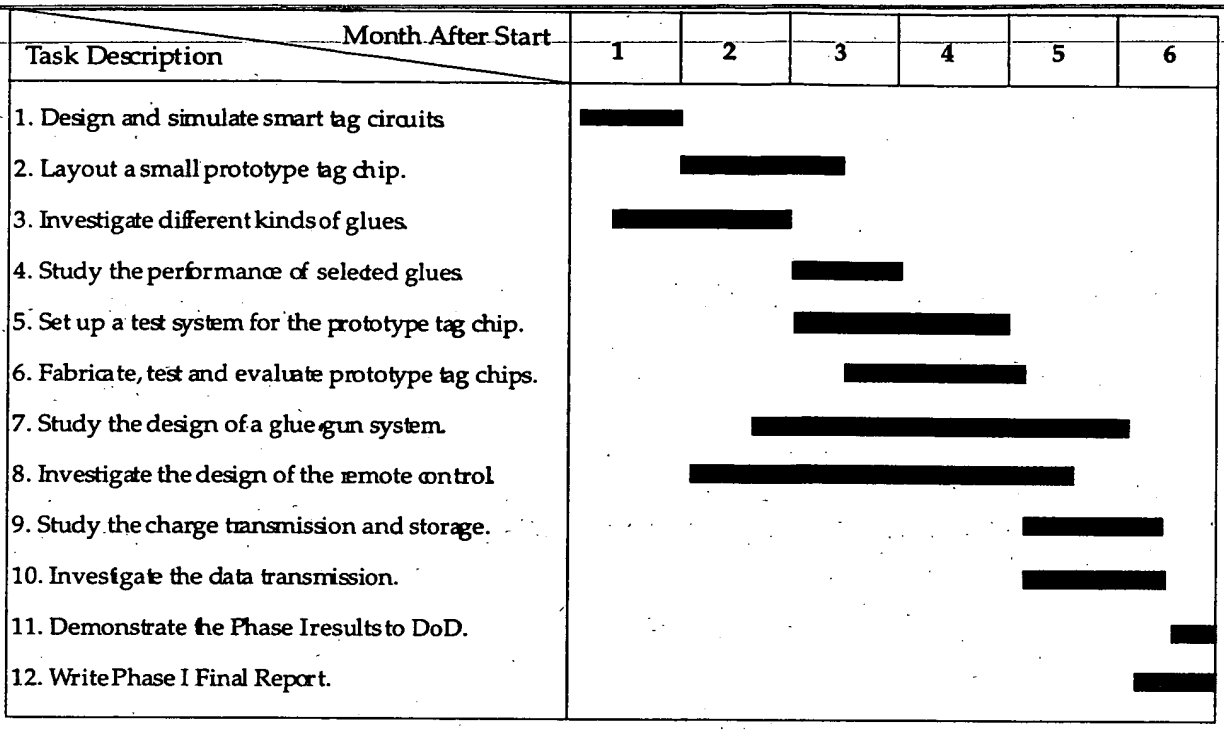
The proposed task schedule for Phase I is shown in **Time-Line Chart.**

Time-Line Chart for Phase I Tasks



C. PHASE I WORK PLAN

C. 1. Introduction

In this section the three parts of this project, tag, remote programmer/reader and applicator will be discussed. Main emphasis will be placed on the tag electronics which is, by itself, the most important and difficult component of the whole system. The design and development of a prototype remote programmer/reader will be carried out in Phase II but a preliminary design will be prepared during Phase I.

C. 2. Antenna Circuit for the Smart Tag

The antenna circuit is the most important section of the proposed tag chip. It will be designed to receive the maximum possible power from the remote programmer/reader and store it onto a capacitor for use by the tag for receiving signals, recognizing and storing the data into memory and transmitting data back to the remote reader.

The receiver/transmitter circuit may be formed from a closed loop antenna with several turns running around the perimeter of the integrated circuit. The antenna will be attached to a parallel LC tank circuit (**Figure 1**). This circuit forms its highest impedance at the resonant frequency of the LC tank circuit so the transmission/receiver wavelength will be set to this frequency.

Other antenna types such as dipole, half wave, quarter wave, etc. will be carefully studied and simulated. Each antenna type has its own benefits and problems. The simulations will help the selection of the best antenna type for the proposed system.

Antenna placement onto the tag chip may have a lot of potential problems that must be avoided.

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One of these is the width of the antenna line. It must be carefully optimized as the adjacent layers can be electrically shorted to form a single line. The thickness and width of the antenna line should also be kept as large as possible. Since the aim is also to produce the smallest chip area, a compromise must be made that will work. Three dimensional simulations of the antenna system will be used to accomplish this.

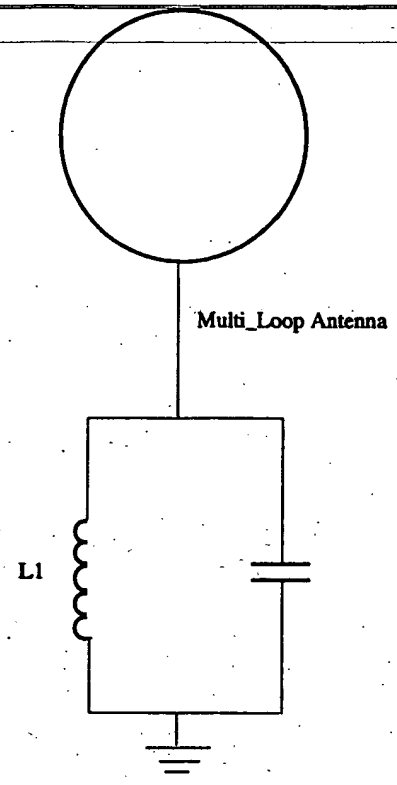


Figure 1. Parallel tuned antenna circuit.

The efficiency of a loop antenna is related to the area as the fourth power and the induced current squared as given in the formula below.

C. 3. Transmitting through a Small Circuit Loop Antenna

The radiated power from a loop antenna can be obtained (Ramo, Whinnery and Van Duzer, 1965) by the integration of the time averaged Poynting vector which is the power density at any point.

$$\vec{P} = \vec{E} \times \vec{H}$$

In the spherical coordinates, the total power radiated is

$$W = \int_0^{\pi} \int_0^{2\pi} P_r r^2 \sin\theta d\theta d\phi = \int_0^{\pi} \int_0^{2\pi} K \sin\theta d\theta d\phi$$

where P_r is the radical component of the Poynting vector and K is defined as the radiation intensity. For a loop antenna, K is obtained as

$$K = \frac{\eta}{8\lambda^2} k^2 \pi^2 a^4 \sin^2\theta = \frac{\eta}{32}(ka)^4 I^2 \sin^2\theta \ .$$

The power radiated by the loop antenna is,

$$W = 2\pi \int K \sin\theta d\theta = \frac{\pi\eta}{12}(ka)^4 I^2 \qquad (1)$$

where a is the radius of the loop, η comes from the impedance of media and k is the wave constant.

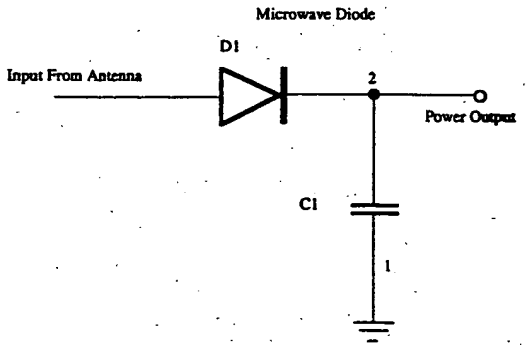
C. 4. Rectifier Circuit

The microwave power received by the antenna may be rectified by the action of a single phase rectifier (**Figure 2a**). The rectifier is a silicon diode specially designed for microwave frequencies. A diode design has to take into account the diode layout on silicon to avoid the power being coupled past the diode by the parasitic coupling capacitance of the layout and the diode. A single phase rectification is fairly simple and involves only one diode drop through the diode to lower the available voltage from the radiated source. Full wave rectification may also be used as discussed below to increase the power stored.

The charge storage capacitor will be designed to be as large as possible (≥ 1,000 pF) to store sufficient energy to power up the circuit. The amount of energy stored is related to the peak electric field in the vicinity of the antenna.

A full rectifier is also feasible to implement on the tag chip (**Figure 2b**). This circuit has the disadvantage of having a two diode voltage drop, but makes up for this by allowing power storage from both the negative and positive swing of the received RF waveform. This circuit is also more difficult to layout for correct operation at microwave frequencies. The correct achievement of this will require a careful three dimensional model of the electric fields to prevent RF coupling from bypassing the special microwave diodes.

a)



b)

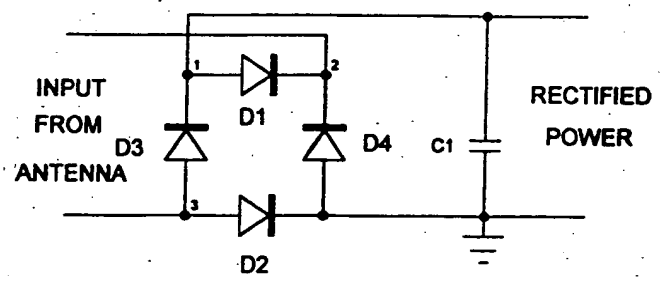


Figure 2. a) Single phase rectification and b) full wave rectifier for the power storage onto capacitance C1.

A reasonable size capacitor achievable on a small layout will approach 1,000 pF depending on the oxide thickness. Typical CMOS processes in modern laboratories are achieving 250 angstroms oxide thickness. This makes 1,000 pF capacitor fairly easy to manufacture. Capacitance stores charge according to the familiar

$$Q = CV$$

relationship. A charge of 10,000 picocoulombs will be present if the capacitor is charged to about

10 volts. One micro amp of current could be provided for 10 millisecond from this much stored charge. All the charge will not be provided at 10 volts during this time if a steady current at this value was drawn from the capacitor. The total integrated circuit will be designed to operate using minimal power. Techniques to keep the power usage low are to use split threshold voltages (Vt). A higher threshold voltage will be used on standby current circuits. A lower threshold voltage will be used on dynamic circuit MOSFET's. A lower power is achieved in the digital section if the ratio in transistor sizes is optimized toward power consumption. CMOS inverters typically are designed to center the switch point and equalize the rise and fall times between the N and PMOS devices. But power is minimized by using less gate area, sizing for drive required from each stage, and reducing the cross over conduction during switching. A total average circuit current of 100 nanoamp will be a system goal for operation of the tag circuit. Burst current for transmission will be much higher, but the system interface could recharge the system for a brief time after each transmission.

A two antenna system, where one tuned for receiving power and the other tuned for receiving and transmitting data will be studied and simulated. If such a system is found to be feasible then the chip could be receiving continuous power while receiving and sending data.

C. 5. The Description of the Complete Tag System

The complete tag integrated circuit chip is shown in a system block diagram in **Figure 3**. Each section is shown with a label for its function and the connection to other sections through the data path(s).

Received microwave power is rectified and stored. The rising voltage on the power capacitor will cause the chip to turn on when a sufficient amount of charge is received to activate the system clock and power on reset. After a number of clock cycles the chip is fully charged and a valid read or write signal sent by the remote programmer/reader module is detected by the band pass filters. These filters produce an output which is an analog voltage, if the voltage level is sufficiently high, a power valid signal is sent from the comparators. The read/write flip flop is then latched to reflect the detected state.

The read or write signal is also sent to the chip control section and the memory. The control steps through a set of states reflecting a read or a write cycle. After the read or write cycle the latch is cleared and the chip looks for another read or write signal from the remote programmer/reader.

The reply code is a special section designed to give each chip a unique reply word. This word tells the remote programmer/reader the circuit is ready to be written to or expect to transmit data. The system interface of each chip will be designed to have about one third of a second to interface with the remote programmer/reader. This time is reduced by the time required to power up the chip. Allowing 200 milliseconds for the chip to charge leaves 130 milliseconds for communication.

This 130 milliseconds is the time allotted for the chip to run through its control routine and several read/write cycles. A 100 kHz system clock will complete 13,000 cycles in the allotted time. Careful use of this time and on chip power management by the control section will allow adequate time for several read/write cycles at a conservative rate to verify proper chip information and that the data is correctly stored.

An electrically erasable programmable read only memory (EEPROM) is selected as the most suitable memory for the tag chip. An EEPROM offers non volatile and reprogrammable memory. Different kinds of EEPROMs and other memory circuits will be investigated for application to the proposed tag chip. New ideas will be also investigated and simulated. The circuit which requires the least power to write and read will be selected.

The tag chip will be reprogrammed on activation by the transmission of the write code. A control section will activate an on chip voltage multiplier and boost the write voltage up to the correct voltage when the write mode of operation is received. The memory will be organized as a 10 to 1,000 byte cell depending on the available power for the prototype chips. For production version tags the memory size is expected to be a few thousand bytes. If writing into the memory becomes a

major power drain then highly encoded and compressed data will be used to reduce the memory size to a manageable level.

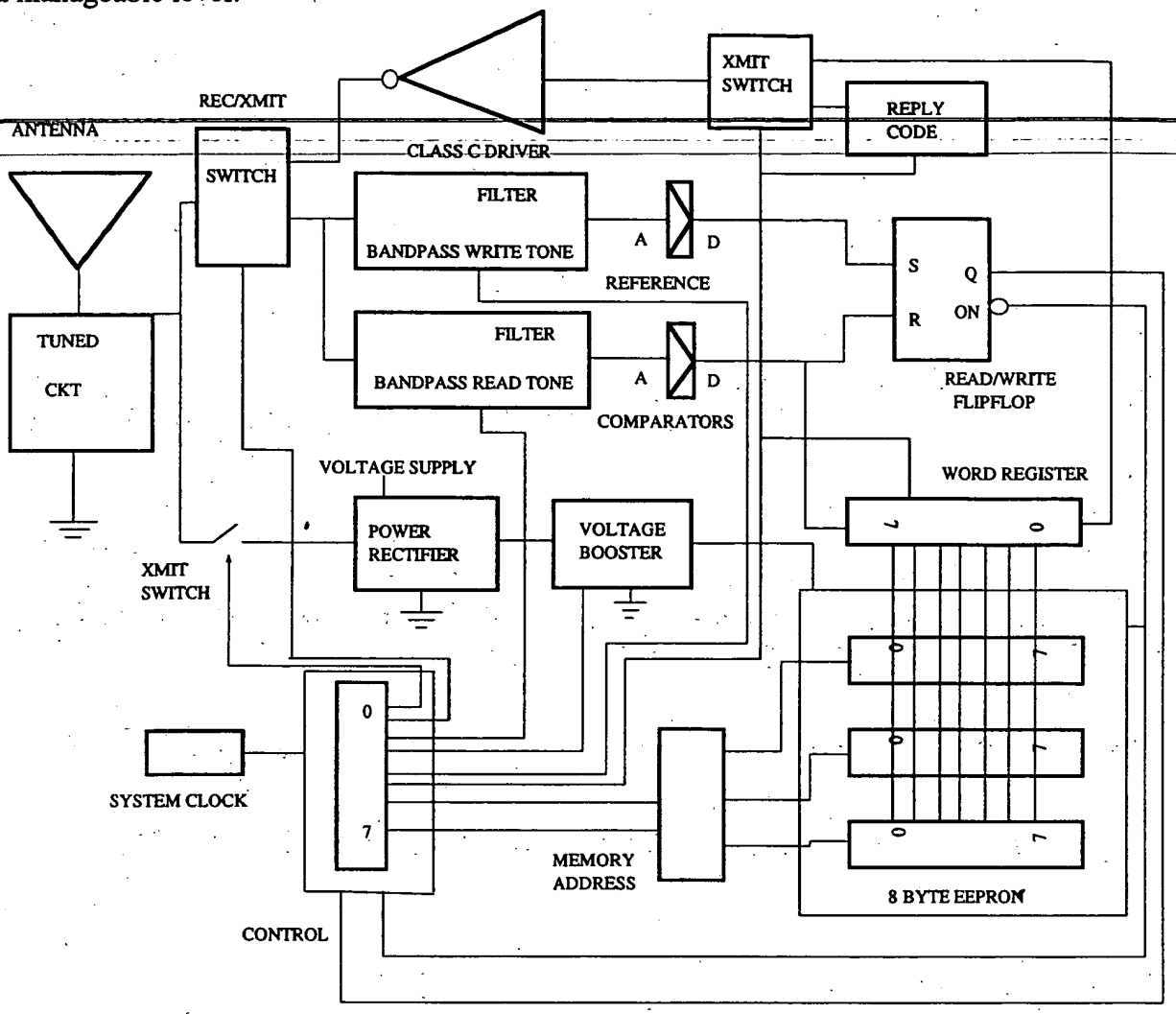


Figure 3. The complete system block diagram of the tag chip.

The control section will be a small state machine. The clock will sequence the operation of the state machine after the circuit is initiated when the registers are cleared by the power on reset circuit. The sequence of operation from the state machine will be sent to the read or write mode by the reception of the read/write signal from the bandpass filters. After valid detection of the read/write bit, the circuit will begin a valid read or write operation after sending back an acknowledge signal informing that it has accepted the command from the remote programmer/reader and the requested operation will be initiated.

C. 6. Bandpass Filters

The bandpass filters are tuned filters to demodulate a tone from the high frequency microwave signal. This tone will be interpreted into a read/write signal. These filters are envisioned to be pretuned to widely spaced frequencies during processing. The filter frequencies are chosen to prevent harmonic overtones of one frequency from coupling falsely into the other pass bands. A passive high frequency rejection filter keeps the microwave power from entering the input of the filter. A blocking capacitor keeps the input bias point decoupled from the RF section. A CMOS op amp with active bias control is used to give low power operation. After valid signal detection from

the remote programmer/reader one or both (if the circuit is set to read mode) of the filters will be powered down to reduce power consumption.

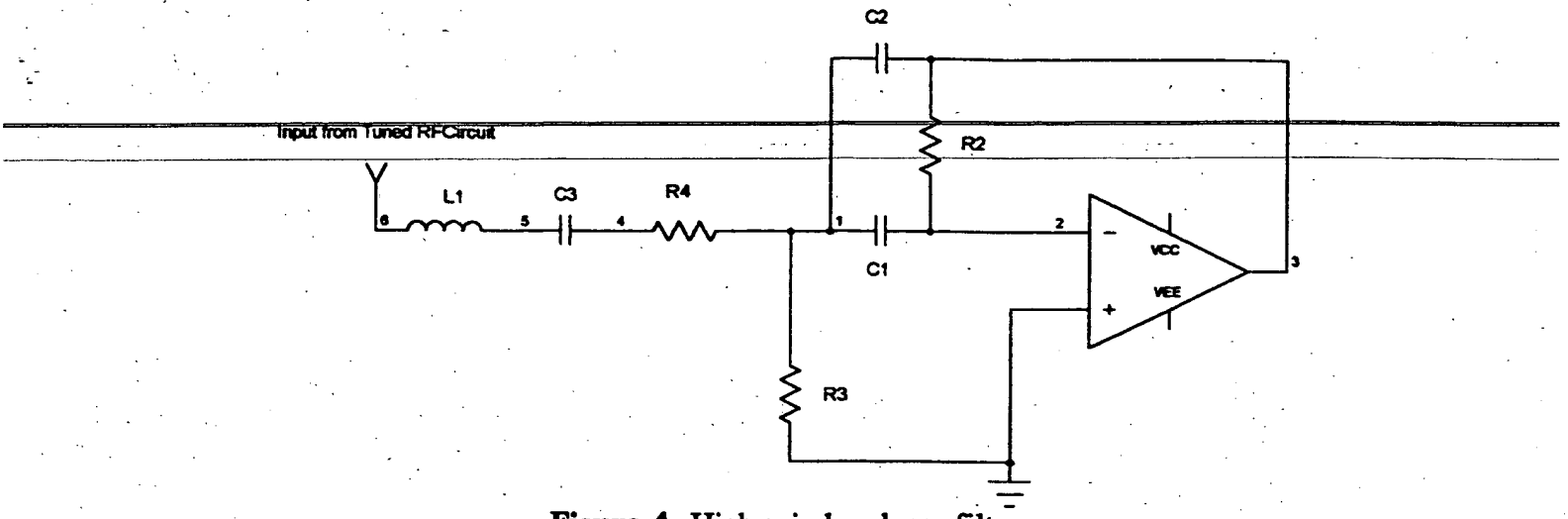


Figure 4. High gain bandpass filter.

The output of the filters will be sent to a CMOS comparator which will latch high or low if the signal level is above the reference level. The output of the comparator will determine the write or read mode for the tag chip. These filters will be an important part of the circuit. They will be fully simulated and optimized. They will be powered up at the end of each write/read cycle to detect the next command.

C. 7. Master System Clock

The master clock for the tag chip will be designed around a simple 3 stage inverter circuit (**Figure 5**). The operation frequency is determined by the resistors R1, R2, and capacitor C1. The frequency of operation can be set during processing and will vary about 10 to 15 percent depending on the variation of the process parameters. A 1 MHz clock speed could be achieved if the values for R1 and R2 are set to 22 KΩ with C1 adjusted to 9.9 pF. This clock speed is fairly high and less power will be used by the clock circuit if the resistors are set to 200 KΩ. This will reduce the clock speed to the 100 kHz range. Analysis and simulation of the overall system will determine the best frequency to use. Since the system is independent and asynchronous the variation in the operation speed will cause no problem for the read/write system.

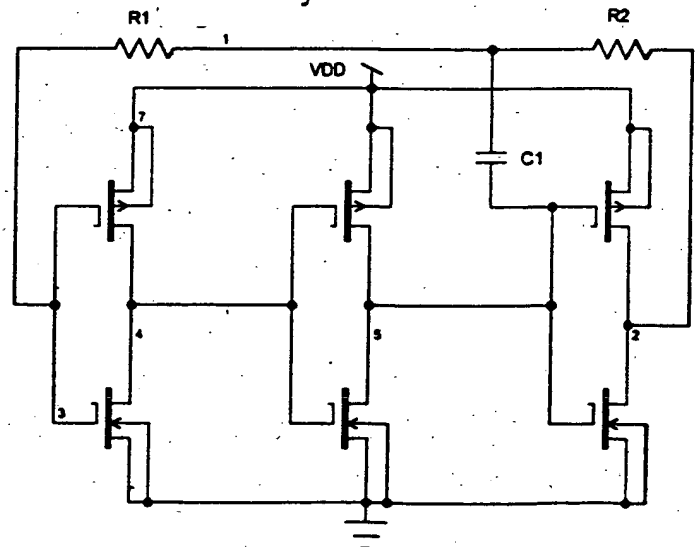


Figure 5. Three stage master system clock circuit schematic diagram.

C. 8. Transmitter Circuit

In the transmitter circuit (**Figure 6**) the transistor is operated in the burst mode. This mode of operation is known as Class C. The operational efficiency of such a circuit can be as high as 90 percent. The NMOS driver transistor excites the resonant circuit into oscillation by the sudden application of a current pulse. The pulses of current are applied at regularly spaced intervals. Therefore, a missing pulse will be detected by the interface system as a logical zero. A changing pulse sequence will represent the serial logic output of the information from the EEPROM memory. Transmit operation will be alternated with receive operation by the use of control logic from the state controller. This control gate is illustrated as ANT_CTRL and ANT NCTR in the schematic diagram of the transmitter amplifier. Each transmit operation will be signaled by a series of closely spaced pulses called the reply code. The interface system will already be in a wait state after time out of the charge sequence and the sending of the read signal. If transmission signals are not detected after a fixed time the read signal will be repeated and another fixed wait state will be initiated. The elements of the transmission circuitry are shown in **Figure 6.**

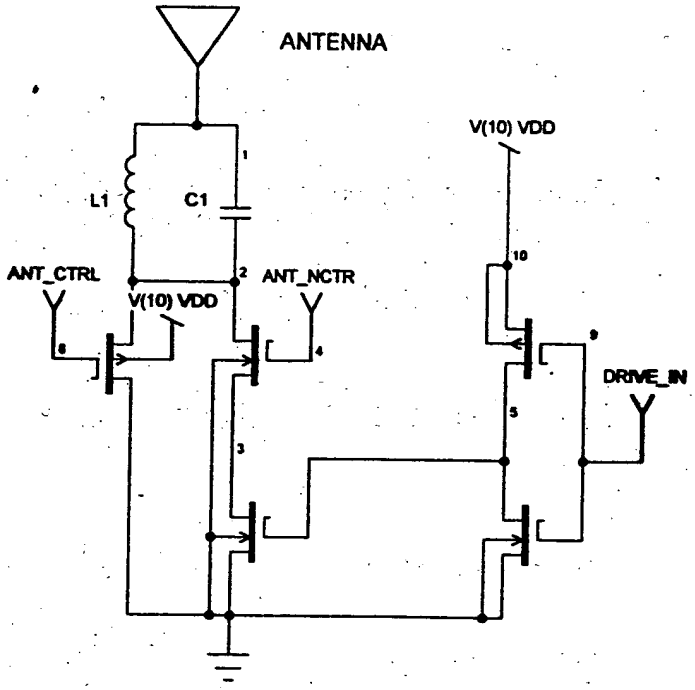


Figure 6. The schematic circuit diagram for the transmitter circuit at transistor level.

C. 9. Receiving and Transmitting Circuit

The receiver interface for the microwave tag system is a high gain antenna with a reception angle over 90 degrees. The front end will be designed to be a low noise receiver detecting the transmission pulse from the tag integrated circuit. The pulses of microwave energy will be similar to the pulse of a strobe light in a visual system. The average power used by the transmitter will be quite low, yet the peak power in each pulse can be quite high. In the low power system of the tag the transmit current of 1 micro amp will utilize at least 1 percent of the stored charge. The transmission of 40 pulses will utilize 40 percent of the stored charge for a 10 volt 100 pF system. A calculation of radiated power from a loop antenna using the equation (1) derived in **Section C3** is conservatively based at 200 femto watts for each pulse at a 10 GHz resonant frequency. The power efficiency improves quickly as both the area of the loop and the wavelength is increased. This calculation is done for a loop radius of 1,000 micrometers. A ten fold increase in loop radius brings the transmitted power up to 2 nanowatts at the same frequency and loop excitation current.

Detection of the signal is dependent on the background radiation and the extraneous noise. Careful choice of the reception frequency will be part of the system design to put the center frequency in an interference free wavelength region. The ambient microwave noise background is related to temperature and the bandwidth of the receiver. If the interface receiver is designed for a very narrow bandwidth of 1 MHz, the total thermal noise power is approximately 4 femto watts. Thus the system will have a signal to noise ratio of 50 based upon the small radius antenna of 1 millimeter length. A 1 centimeter antenna will have a signal to noise ratio of 500,000. Therefore, based on these simplified calculations, a system antenna with a loop radius of 3 millimeters will give a signal to noise ratio of 4,000. These theoretical calculations are based on signal power at the emitter or transmitter. Any reduction of power at the receiver will be related to the total angle of transmission, and the distance from the source proportional to the inverse of the distance. Therefore, it will be designed to receive and transmit without any preferential direction, to allow the tag chip to have an arbitrary orientation.

C. 10. Voltage Booster Circuit

Upon reception and verification of a valid write signal, the control section will activate the voltage booster circuit. This circuit is designed to charge a stack of capacitors in series at a low voltage. This series stacking is achieved by means of a combination of capacitors and diodes organized as shown in the voltage booster schematic circuit (**Figure 7**). In action the system clock is used to charge the three capacitors in an alternating fashion to multiply the clock voltage to a voltage high enough to bias the write voltage and inject charge into the floating gate electrodes of the EEPROM array. A one or a zero can be written to a memory cell site by application of the write voltage and the address byte.

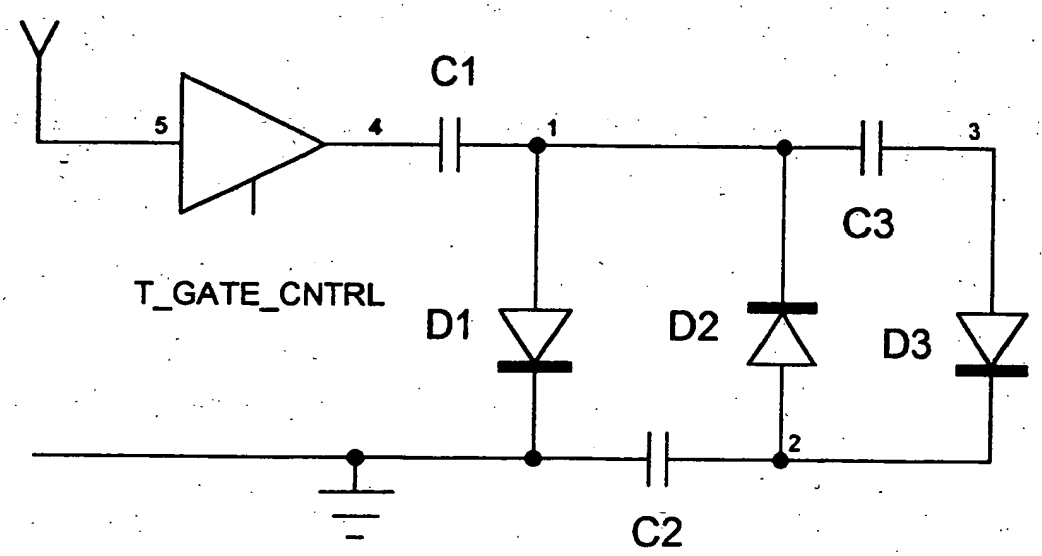


Figure 7. Voltage Booster schematic circuit diagram.

C. 11. CMOS Comparator Circuit

Each bandpass filter provides an analog output depending upon the magnitude of the signal received. In order to have this signal drive digital logic it must be latched to a high or low DC level. This function is accomplished by the CMOS comparator. This circuit is illustrated in **Figure 8**. The input stage is composed of both N and PMOS feedback loops which determines the switching level of the comparator. The circuit achieves this adjustment through varying the MOSFET width to length ratio. These values are determined through computer aided simulation of the circuit operation. This circuit is simple and it is process insensitive. It does not require the use of a separate reference generator. These are all key benefits for the low power requirements of the tag electronics.

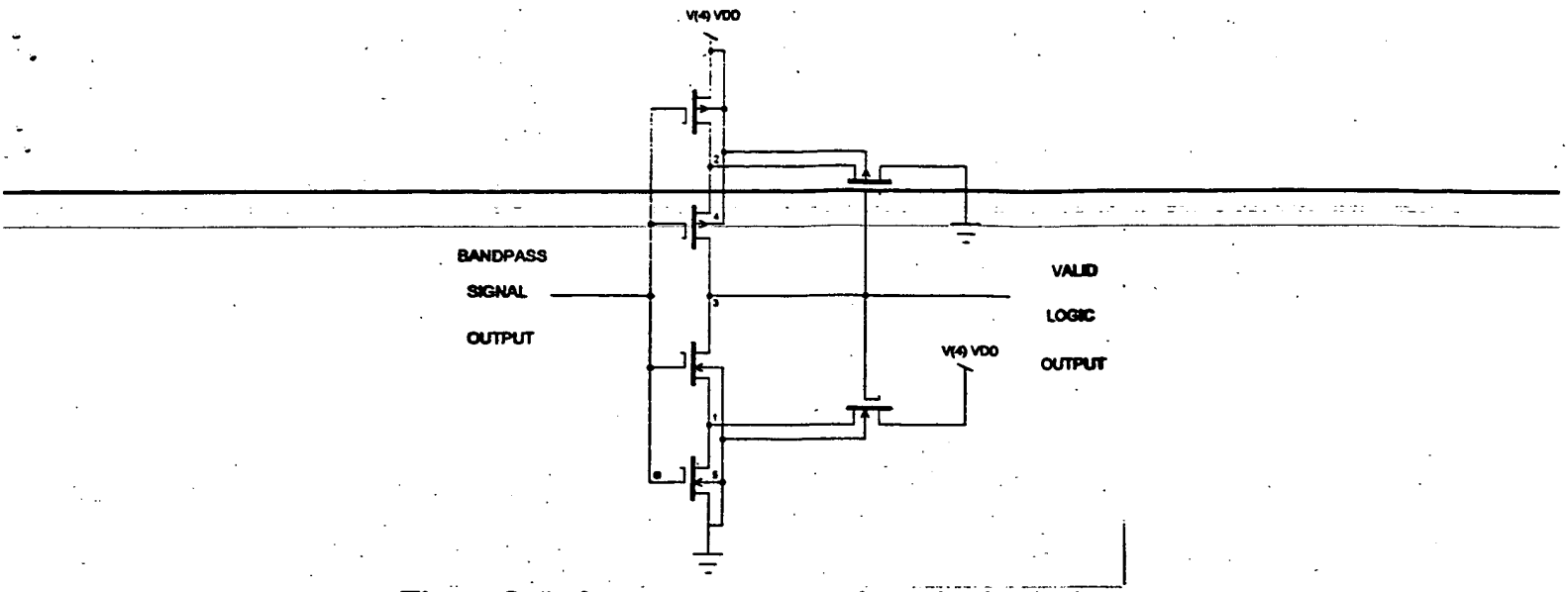


Figure 8. Reference comparator schematic circuit diagram.

C. 12. Control Logic Organization

The control register (**Figure 9**) is organized as a state machine which is sequenced by the system clock. The start pulse is launched into a D type flip-flop shift register which is cleared by the power on the reset function after the system clock is activated. A start signal is received from the valid logic detector after the bandpass filter detects a read or write tone signal. The organization of the control register is shown for a valid control word 1, 2, 3... The output is picked from the transmission gates by the CTRL lines 1, 2, 3... (Only one cell is shown in **Figure 9**.)

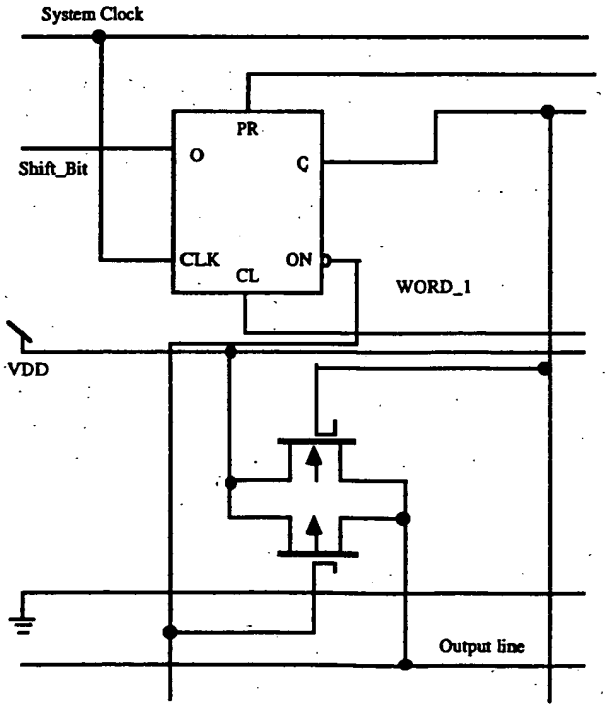


Figure 9. The control logic register (only one cell is shown).

The control register continue to switch in and out the control words as the D shift register is incremented. At the end of the register the sequence is started to open the bandpass filters for detection of another control command from the interface system.

C. 13. EEPROM Memory Organization

The EEPROM memory (**Figure 10**) is organized to read and write under the address control. A single cell of a core memory is shown in **Figure 10**. The EEPROM cells are MOSFETS with the extra floating gate controlled by the ROW LINE. In write operation the appropriate column is selected by the column multiplexer. After selection the row line is pulsed to erase all the cells to zero. A one can be written to the appropriate cell by selection of the row select line. The high voltage switch is enabled and a high level signal is applied to the drain of the MOSFET selected for write. The MOSFET stores a one when it is selected. In read operation the cell is addressed by the row and column registers. Each column will be high corresponding to a stored zero and low corresponding to a store one. The sense amplifier and logic creates the correct output sense for positive logic.

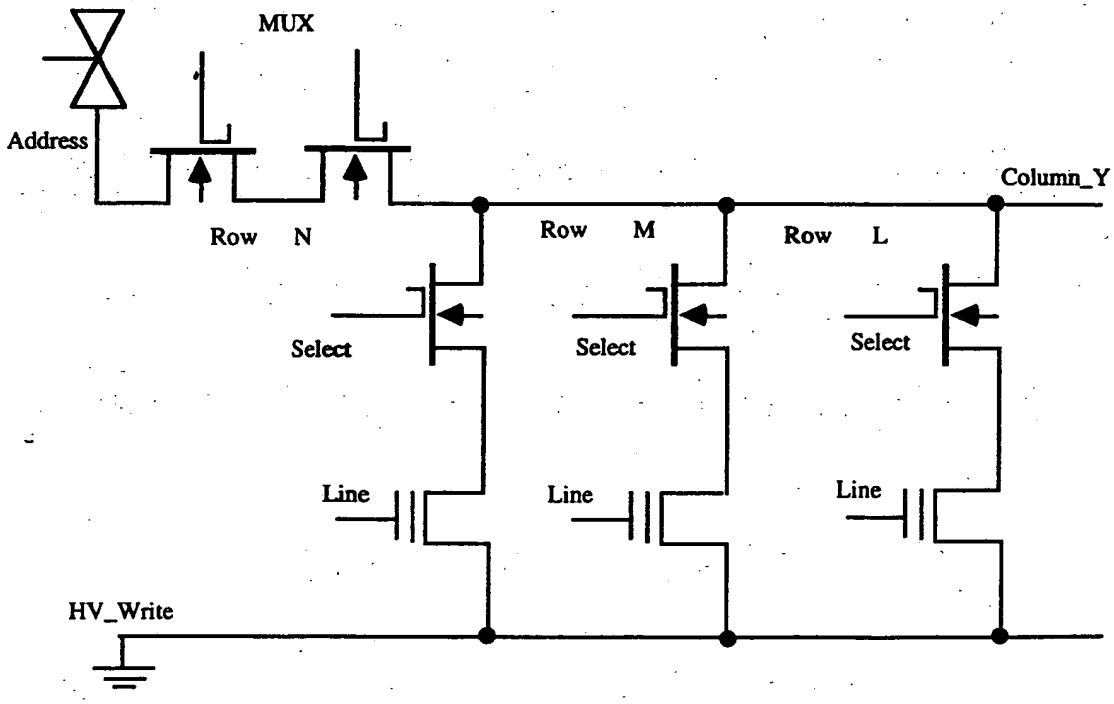


Figure 10. The EEPROM memory circuit (only one cell is shown).

C. 14. Estimated Total Power Dissipation

The total chip power is dependent on the size of the memory, the amount of control logic and the speed of operation. An estimate of the total power dissipation can be calculated using the power per gate and the number of gates (**Table I**). For the tag chip the amount of memory in the prototype Phase I circuit will be smaller than for the Phase II work. We will discuss here the small Phase I prototype chip.

A typical memory cell is composed of six transistors. The number of cells of this type are in the temporary registers used for data load, addressing and control latch. The control logic will be built into a fixed ROM based state machine with virtually no power dissipation. One program routine is reserved for the read operation and the second program routine is designed for the write operation. Therefore, a one or zero of the appropriate register will be placed on the control output bus by sequencing through the control shift register with the system clock. An approximate estimate has

been made of the amount of logic to operate the entire tag integrated circuit. This estimate assumes a basic eight bit word and an eight bit control logic.

Table I. Preliminary tag chip component count.

Ten step shift register	160 transistors
Control array 8 bit byte read operator	240 transistors
Control array 8 bit byte write operator	240 transistors
Master clock	6 transistors
Reference comparators	12 transistors
Four latches (8 bits each)	480 transistors
Transmitter	6 transistors
Operational amplifiers in bandpass filter	24 transistors
EEPROM memory 64 8 bit words	200 transistors
Assorted individual gates	60 transistors

This rough estimate indicates a tag circuit with a 64 byte storage and a read and write control section has on the order of 1,500 transistors. Thus a total inverter count of approximately 750. The total chip power estimation will be made using the following formula (Davari et al., 1993) with an average capacitance C_L per stage of 0.02 pF and a clock frequency F_{clk} of 100 kHz.

$$P_{total} = P_t(C_L V_{dd}^2 F_{clk}) + I_{sc} V_{dd} D_t + I_{leakage} V_{dd}$$

The first term in this equation is the dynamic power dissipation. The second term is the direct short circuit current as the inverter switches in the CMOS logic. The last term is the DC leakage current for the CMOS gate. The power is calculated in watts. P_t is the activity factor which relates the switching activity of each section circuit function. We will assume a 0.5 activity factor. V_{dd} varies but our calculation will be for 3 volt logic. The leakage current for a typical stage is 10^{-14} amps. The I_{sc} which is the short circuit current can be tailored to be low by optimizing the gate design to minimize the overlap time of the on times for the PMOS and NMOS transistors. D_t is the duty cycle of the short circuit current. A value of 10 nanoamps for I_{sc} and 0.1 for D_t is assumed. Total power dissipation is estimated at 12 nanowatts. Total power available is 300 nanowatts. These calculations indicate a feasible tag circuit within the constraints specified.

C. 15. Smart Tag Applicator

The applicator will place a smart tag onto the surface of a baggage. It can be placed on the top (or side) of the x-ray scanner downstream from the x-ray tube as shown in **Figure 11**. The automatic baggage inspection system will decide which baggages need to be tagged right after that baggage pass under the x-ray tube. Generally, only those baggages which trigger the automatic baggage inspection system will be tagged. However, if needed all packages can be tagged. In such a case the tags can be applied prior going through the x-ray scanner and only programmed after passing the automatic inspection system.

The preliminary proposed structure of the applicator is a glue tank, a piston, and an air valve (**Figure 12**). The tag chips can be mixed into the glue prior to connecting to the applicator or it can be mixed in the applicator. The glue-tag combination will be sent to the small chamber below the air valve (marked B). The operation of the pressurized air will 'shoot' the glue-tag ball down onto the surface of the baggage. An LED with a photodiode can be used to verify that there is a tag chip inside the glue ball at the mixing (A) or shooter (B) chambers. This will be studied during Phase I.

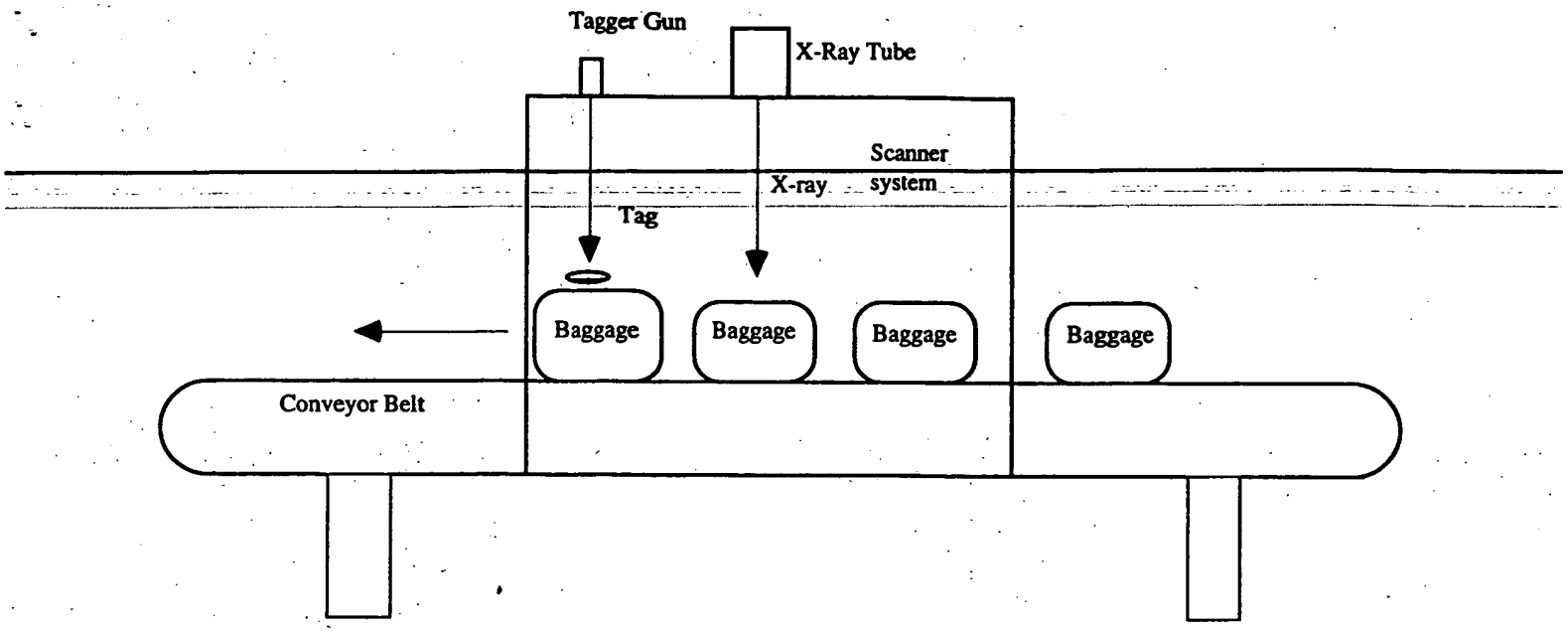


Figure 11. The side view of the x-ray scanner with smart tag applicator.

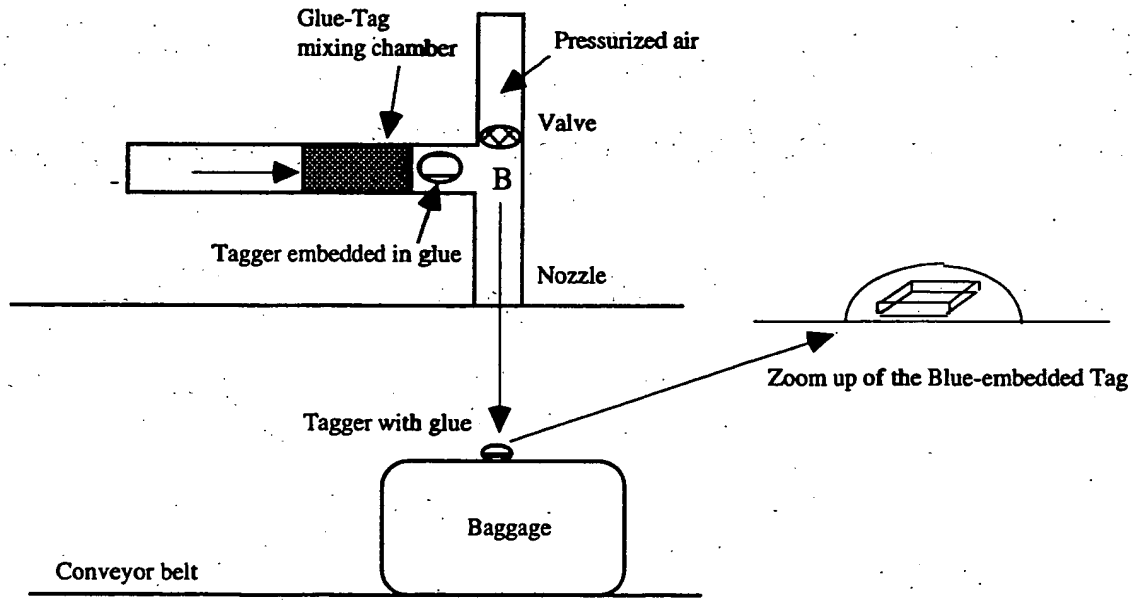


Figure 12. The concept for the applicator mechanism (front view).

The mechanism of transferring the glue-tag combination from the mixing chamber to the area underneath the air valve can be a piston or another mechanism. This will be investigated. As mentioned above the tag chip can be embedded into the glue inside the applicator using a tape conveyor carrying the tag chips at regular intervals similar to those used for transporting surface-mount components. The tag chip is then dislodged from the tape and embedded into the soft glue by the pressure of the glue or using the piston.

The top view of the glue gun concept is shown in **Figure 13**. The LED and the photodiode sensor (**Figure 13**) are used to verify that the glue in chamber A has an embedded tag chip. This

will make sure every motion of the piston will push a tag chip into the chamber B. Pressurized air is applied into chamber B while the electronically controlled piston seals the chamber to propel the glue-tag ball onto the baggage.

Commercially available components will be used for the tag applicator as much as possible. It is expected that some modification needs to be made. If necessary the applicator will be custom designed in Phase II using the results obtained in Phase I. The results of this work will be presented and demonstrated at the end of the Phase I project.

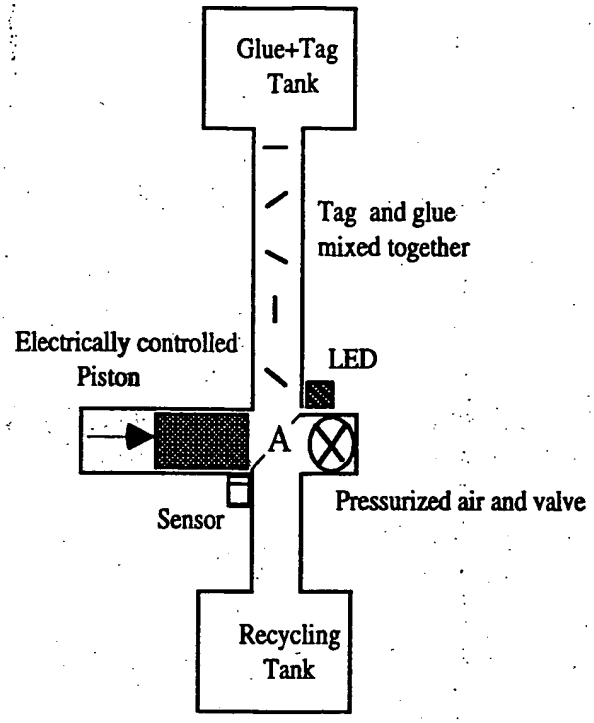


Figure 13. The concept for transferring the glue with embedded tag chip into chamber B (top view).

D. REFERENCES

Ramo, S., J.R. Whinnery and T. Van Duzer, "Field and Waves and Communication Electronics" Published by John Wiley and Sons, 1965.

Davari, B., et al., "Low Voltage Low Power Devices" IDEM, 1993.

E. RELATED WORK

NOVA is developing state-of-the-art mixed signal multi channel ASIC chips for room temperature position sensitive solid state detectors such as silicon and CdZnTe strip, pixel and pad arrays. These detectors with their readout electronics are developed to replace scintillator counterparts for application to industrial and medical imaging.

Five projects are presently under development at NOVA. The industrial projects are now in the Phase II stage where engineering prototypes are being built. The first project is a space based gamma ray detector for the detection and discrimination of nuclear warheads from decoys deployed by intercontinental ballistic missiles. A mixed signal (analog and digital) ASIC front-end readout (RENA) chip with 32 channels is also being developed to read out the new silicon strip detectors for this project. This chip is now in commercialization phase. An improved version is being fabricated. This chip has been designed to be versatile and flexible. It can be applied to most solid state detectors such as the CdZnTe strip or pad detectors without modification.

The second project is a nondestructive imaging inspection system for large and dense objects using x rays. Both projects use silicon strip detectors. A derivative of the second project is also started. It is an automatic baggage inspection system for USDA and FAA, a linear pixel CdZnTe pad detector array with 1 mm pitch (active area 4 mm x 32 mm) and a 32 channel fast mixed signal ASIC (FESA) chip for reading out these detectors are being developed. The first prototypes have been fabricated. The ceramic carrier, electronics and test station have been made. The experience gained on the development of the FESA chip will be important for this project.

There are two major medical projects progressing at NOVA. The first project is the high sensitivity single photon emission computed tomography (SPECT) system. The second medical project is a high resolution digital mammography system. Both projects have been funded by NIH. Solid state detectors such as silicon strip, CdZnTe pad and silicon pixel detectors are used in these projects. The design of a prototype pixel detector with its dedicated readout ASIC chip has been developed and tested. This is a charge integration type mixed signal ASIC chip with TDI capability different than the other ASIC chips. We are now designing the second, full scale, version of this chip. This new front-end readout chip will bring new capability to NOVA's solid state detectors. The experience gained on this third ASIC chip will be also important for the proposed project.

Two more proposals were recently funded. They are for a new high sensitivity scintimammography system and a CdZnTe pixel detector based high contrast digital mammography system. All these projects are based on solid sate detectors with custom mixed signal ASIC readout chips.

Also, NOVA has finished the development of a portable hand-held narcotics detector under an SBIR Phase II contract with DOT/Coast Guard. The prototype unit has recently proved its capability by being instrumental in detecting several concealed large narcotic drug shipments. The Phase III marketing of this detector is in progress in cooperation with our Phase III sponsor. This shows that NOVA is striving to carry out research and development with the sole aim of bringing state of the art products into commercial market.

F. RELATIONSHIP WITH FUTURE R&D WORK

F. 1. Anticipated Results of Phase I and Phase II

The results of Phase I and Phase II work will be the development of a commercial smart tag system with remote controller and applicator. The tag will be manufactured on silicon and will be completely self contained not requiring any external antennas or batteries. It will have very small size and will be programmed and readout by a remote controller within a distance of $\geq$ 1 m. An applicator is proposed that will place the tag on the item inside a tiny non hardening glue ball which can be removed without affecting the surface of the item it is attached to.

F. 2. Significance of Phase I Work on Phase II Study

This project is proposed as an introduction to Phase II. During Phase I a small prototype will be designed, simulated, fabricated and tested. Therefore, the feasibility of the proposed smart tag system will be experimentally demonstrated. The results obtained from Phase I prototype will save valuable time during Phase II for developing the final commercial product. The applicator will be studied carefully and some experiments will be carried out. These results will be used to develop a commercial smart tag system during Phase II. During Phase III the completed tag system will be manufactured as a commercial product and supplied to government and commercial sectors. Phases II and III are estimated to take two years each to complete.

G. POTENTIAL POST APPLICATIONS

G. 1. Commercial Application

Potential commercial application of a smart versatile tag is self evident and extremely good. It can be applied to monitoring, tracking, searching, labeling, personalizing, selecting and finding

items that belong to a large group. Due to the low production cost the proposed radio frequency smart tags can be used to tag a large number of items without need to recover them. They can also be used in smart card type systems where access to the card can be done remotely. Potential civilian uses of the smart tags include: tagging luggage, bags, boxes in airports; monitoring parcels, packages, crates, and individual items during transport; identifying employees and vehicles; labeling and searching folders, files and dockets; personalizing and recording information on smart cards; tracking inventory; and monitoring merchandise.

The first deployment is expected to be in airports where there is a major need for smart tags by USDA, FAA and the US Customs. The use by airtransport companies for FAA and USDA alone can reach millions of tags per year. When all the other sectors are put together the ultimate use of the smart tags may approach a billion tags per year.

The smart tag is straight forward to manufacture once the working design is completed. It will be fabricated in the form of thousands of wafers in commercial silicon chip foundries . They can be diced immediately since expensive wafer probing to select good chips is not necessary. At this stage NOVA can take over the dies and pass them through a pre-assembled conveyer belt type automatic test and selection system. The bad tags will be diverted and the good ones will be coated for protection and stored for shipment. Such a setup does not need major equipment and funding and a small high tech company like NOVA has the means to carry out this setup with reasonable venture capital funding. The potential of the smart tag is so well defined that once the technology is demonstrated finding venture capital is not expected to be difficult.

The development of the remote programmer/reader and the applicator provides a complete solution to the user. Although these will be shipped in smaller quantities compared to the smart tag they are also expected to bring major income to NOVA.

G. 2. Federal Government Use

The proposed radio frequency or microwave smart tags and applicator can be used for military and other Government applications also. These applications will be quite similar to the applications listed above. For example, some possible military applications include tagging individual weapons, munitions, pieces of equipment, crates, and other inventory. The Government sector is expected to be an important customer for the smart tag system.

H. KEY PERSONNEL

H. 1. General

The key personnel include Dr. Jianping Peng (PI), Dr. Tümay O. Tümer (Co-PI), Dr. Scott Kravis and Mr. Rene Brown. They are all engineers with both chip development and mechanical design experience.

Dr. Jianping Peng (PI) is an engineer at NOVA R&D, Inc. He is in charge of the Automated Baggage Inspection System (ABIS) project and plays a key role in this project: designing, testing and debugging the FESA (Front-end Electronics for Spectroscopy Application) chips, testing the CdZnTe semiconductor detectors, and producing images baggage on a conveyer belt by mounting the assembly of FESA chips and the CdZnTe detectors into an x-ray scanner. He has an excellent knowledge of electronics and experience in making electronic circuits and signal processors (both analog and digital). He also has the experience in overseeing the IC chip design. He is also developing the ABIS imaging software using C^{++}.

Dr. Peng has a Ph.D. in physics from the City University of New York, and also a M.S. and B.S. in physics from the Peking University (P.R. China.). Before arriving at NOVA Dr. Peng was a research assistant at Brookhaven National Laboratory. His work consisted of research were he performed analysis of particle interaction with solids, particle annihilation, positron and electron

scattering and channeling in single crystals. He also performed research involving ultra-high vacuum technology using mechanical, turbal-molecular, ion, and titanium sublimation pumps. In addition he worked with low temperature technology using a cryo pump cryostat, and cold head. He has also developed the electronics for these projects. He will carry out most of the tasks listed in the work schedule.

Vice-president Dr. T.O. Tümer is the Co-Principal Investigator for this project. He will be responsible to NOVA for the successful conclusion of this project. He has 30 years experience in detector design, development and fabrication. Dr. Tümer has worked at NOVA since it was founded 12.5 years ago. He has over 75 publications in scientific journals and books, and many more reports, presentations and abstracts. He has supervised students and directed many research projects. He has extensive experience in fast electronics, ASIC chip development, gamma ray and particle detectors, Compton double scatter techniques and real-time data analysis. He has also extensive experience in silicon and CdZnTe strip, pad and pixel detectors and their applications. He is the PI of two Phase II contracts, one for DOD/BMDO for a space borne gamma-ray detector for gamma rays from 0.3 to 30 MeV and the other for DOD/Army on nondestructive inspection of munition items with x rays. He is also the PI of two new projects just been awarded on medical imaging; scintimammography and digital mammography. He will oversee the development and commercialization of the proposed smart tag system.

Engineer Dr. Scott Kravis, previous to employment at NOVA R&D, Inc., conducted research on highly-charged ion-atom collisions and photoionization of atoms and ions using synchrotron radiation. He has used and applied many radiation detectors and data acquisition systems. He build interface electronics for experimental control. He has also designed and built a high charge state low energy electron beam ion source (EBIS). He has developed all the electronics for these experiments. He has given oral presentations at international conferences and workshops on these topics. Since he came to NOVA, Dr. Kravis has been working on CdZnTe linear pad detector arrays and medical imaging systems. He is primarily working on image acquisition from these detectors through mixed signal ASIC chips and the testing and evaluation of the RENA chip. He will work on the smart tag chip design and optimization. He will also contribute to the design and development of the test and remote control electronics for the smart tag system.

Mr. Rene Brown founded Lasair Design and is the principal engineer and owner. Mr. Brown has 20 years of experience, 16 of which has been with Hughes Aircraft Company. He has designed circuits in silicon, germanium, and GaAs. He has designed 15 focal plane arrays for various applications. Mr. Brown has been involved in many high speed design projects at Hughes. Previous designs include high-speed ECL logic operating at 200 MHz, complementary JFET logic capable of 80 pico second propagation delays, low noise 3 GHz bandwidth low power amplifiers for CO_2 laser systems, a fiber optic receiver using a GaAs transimpedance amplifier and high speed CMOS logic (100 MHz) for infrared CCD imagers, HgCdTe and InSb detectors hybridized to CCD and CMOS readouts, germanium readouts using JFET circuits for amplifiers and logic, GaAs readout with a capacitive transimpedance amplifier using MESFET devices, and BICMOS readouts with differential or folded cascode preamplifiers. He has designed many digital logic circuits including designs in SOS, CMOS, ECL, and IIL logic. He has also investigated logic designed in Ferro electric, GaAs MESFETS, and germanium JFETS. He has designed analog integrated circuits for radiation hard requirements and has extensive test experience with circuits in cryogenic, gamma and x-ray environments. Mr. Brown has MS BS degrees in electrical engineering from the University of California at Davis. He has authored or co-authored seven papers on focal plane arrays and signal processing for focal plane arrays. Mr. Brown is a registered Professional Engineer in the State of California (E 11255). He will work on the silicon layout of the smart tag ASIC chip.

All members of the key personnel plan to take part in Phase II of this project, are totally committed and are determined to make the proposed project a great success.

H. 2. Resume of the Principle Investigator

JIANPING PENG: *NOVA R&D, Inc.*

Education:	Peking University (P.R. China)	B.S.	1984	Physics
	Peking University	M.S.	1987	Physics
	City University of New York (USA)	Ph.D.	1996	Physics

Professional Experience:

9/89 to 1/92	Teaching Assistantship and Research Assistantship: Dept. of Physics, City University of New York.
2/92 to 12/96	Research Assistantship: Dept. of Physics and Materials Science Division, Brookhaven National Laboratory.
1/96 to Present	Engineer, NOVA R&D, Inc.

H. 3. Related Publications from Past Three Years

1. Vacancy defects in photoexcited GaAs studied by positron two-dimensional angular correlation of annihilation radiation, J.P. Peng, K.G. Lynn, M.T. Umlor, D. J. Keeble and D. R. Harshamm, Phys. Rev. B 50 (Rapid communication), 11247 (1994).
2. Observation of diffraction effects in positron channeling, J.C. Palanthingal, J.P. Peng, K. G. Lynn, X.Y. Wu, and P.J. Schultz. In the Proceedings of the 10th International Conference on Positron Annihilation. 193 (1994).
3. Quantum channeling effects for 1 MeV Positrons, R. Haakensasen, L. Hau, J.C. Chelovchenko, J.C. Palachingal, J.P. Peng, P. Asoka-kumar, K.G. Lynn, Phys. Rev. Lett 75 1650 (1995).
4. Study of the Silicon-Dioxide/silicon interface using variable energy positron two-dimensional angular correlation of annihilation radiation, J.P. Peng, K.G. Lynn, P. Asoka-kumar, D.P. Becker, D.R. Harshman, Phys. Rev. Lett. 76, 2157 (1996).
5. Defects identification using core-electron contributions in doppler broadening spectroscopy of positron annihilation, S. Szpala et al., Phys Rev. B, 1996 (accepted).
6. On the role of classical and quantum notions in channeling and the development of fast positron as a solid state probe of valence and spin density, L. Hau et al., Nuc. Ins. M. B, 1996.

I. FACILITIES AND RESOURCES

Laboratory: The ASIC chip development and testing electronics and detector development laboratory at NOVA R&D, Inc. will be available for this work. The facilities also include state of the art test equipment for wafer probing and wire bonding capability, calibration and evaluation of radiation detectors.

Computer: NOVA R&D, Inc. has many computers available for the simulation and optimization of the detectors. The data analysis and imaging software development can also be carried out. The computers include Unix workstations and top performance IBM-PC and Macintosh desktop computers.

Office: The offices at NOVA R&D, Inc. will be available for this project. The offices include excellent report and paper generation capabilities and an experienced purchasing department.

Major Equipment: NOVA R&D, Inc. has the following equipment available for this project: a Pantak HF-160 x-ray system generates x-ray photon up to 160 keV; nine computers; a logic analyzer, an ultrasonic wire bonder, a wafer probe station, a spectrum analyzer; two oscilloscopes; a multichannel analyzer; a CAMAC crate with controller; an NIM crate; many NIM modules (spectroscopy amplifier, single channel analyzer with pulse shape discrimination

capability, discriminator, ratemeter, a versatile 4 channel logic module, fan-in/out unit, dual channel counter/timer, time to amplitude converter, precision pulse generator with detector pulse output simulation capability); high and low voltage power supplies; GAL and EPROM programmers; electronic measurement devices; high resolution multimeter; printed circuit manufacture system; environmental chambers with temperature and humidity control capability and many home made special detector test electronics and boards. All the equipment will be available for the proposed research without charge.

Additional information: NOVA R&D, Inc. has been involved in developing sophisticated electronics devices, mixed signal ASIC chips and radioactivity detectors since 1984. There is a sophisticated electronics laboratory and a small machine shop. NOVA has laboratory space available for this project and a radiation licence to use radioactive sources and x-ray generators in its research. There are many gamma ray, electron and positron sources available which could be used in the proposed feasibility study. NOVA facilities meet environmental, federal and California state laws and regulations. It has management and support services to supplement the laboratory work. NOVA is currently developing several products . The expertise gained in these projects is expected to help the proposed smart tag system development significantly and expedite its successful completion.

Lasair Design: Lasair Design has excellent facility. The computers used for silicon layout are fully capable of schematic capture, circuit simulation and logic simulation. The computers also have aided design software for layout, schematic capture, DRC (design rule check) and LVS (logic verification of layout versus schematic). The current processors are a setup for advanced computer aided design. The tape outputs are the industry standard GDS-II for integrated circuits or converted for compatibility with Artwork Conversion software to other desirable formats. All the systems include full tape backup, large format monitors, modems and high speed video cards. An E size continuous feed plotter interfaces to the design computers to create 360 dpi color plots to provide visual checking of our design work. A prototype breadboard and fabrication work area is equipped to build up a test printed circuit design as required for final check out of printed circuit designs. This area is also used to test integrated electronics and circuit boards. A computer controlled laser micro machining station provides precision work in cutting sapphire, GaAs, silicon, stainless steel and other hard substances. Lasair Design is in compliance with all state, federal, and local environmental laws and regulations.

J. CONSULTANTS

The consultant is Mr. Rene Brown. His experience is discussed in the Key Personnel section.

K. PRIOR, CURRENT AND PENDING SUPPORT

There is no prior, current or pending support received for the proposed work.

APPENDIX C

U.S. DEPARTMENT OF DEFENSE
SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM

COST PROPOSAL

1. **NAME OF OFFEROR:** NOVA R & D, Inc.
2. **HOME OFFICE ADDRESS:** 1525 Third Street, Suite C, Riverside, CA 92507
   Telephone: (909) 781-7332, Fax: (909) 781-0178
3. **LOCATION WHERE WORK WILL BE PERFORMED:** Same as above
4. **TITLE OF PROPOSED EFFORT:**

A Practical System for a Low Cost Smart Tag and Applicator

5. **TOPIC NUMBER AND TOPIC TITLE:**

A96-009, Low Cost Radio Frequency Smart Tags and Applicator

6. **TOTAL DOLLAR AMOUNT OF THE PROPOSAL:** $99,938
7. **DIRECT MATERIAL COST:**

a) **Purchased parts**	
General supplies (PCBs, electronic components, cables, connectors, etc.)	7,000
Front end read-out chip foundry charge (MOSIS process)	2,800
b) **Subcontracted item**	
Front end readout chip layout (Lasair Design)	24,000
d) **Total direct material**	**33,800**

9. **DIRECT LABOR:**

Principal Investigator - Dr. Jianping Peng, $23 @ 600 Hr	13,800
Co-Principal Investigator, Dr. T. Tümer $42.525 p/hr @ 59 hr.	2,509
Co-Investigator, S. Kravis, $26.50 p/hr. @ 300 Hr.	7,950

10. **LABOR OVERHEAD (G & A Included)**

118.82% (overhead rate) @ $24,259 (Base, direct labor))	28,825

14. **CONSULTANTS:**

a) **Identification**	
Rene Brown - test support for the read-out chip, 30 Hr @ $65 /hr	1,950

18. **FEE OR PROFIT:** 12.5% @ $88,834 (total costs) 11,104
19. **TOTAL ESTIMATED COST AND FEE OR PROFIT:** **$99,938**
20. **TYPED NAME AND TITLE, SIGNATURE AND DATE OF SUBMISSION**

Sezen H. Tumer, President  July 3, 1996

21. a) Has any executive agency of the united states government performed any review of your accounts or records in connection with any other government prime contract or subcontract within the past twelve months? **YES** (5/26/1996, DCAA San Gabriel Branch Office, West Covina, CA 91790-2900, Ph: (818) 918-5922.)

    b) Will you require the use of any government property in the performance of this proposal? **NO**

    c) Do you require government contract financing to perform this proposed contract? **NO**

22. **TYPE OF CONTRACT PROPOSED:** FIRM FIXED PRICE

NOVA R&D, Inc.
1525 Third Street
Suite C
Riverside, CA 92507
Phone: 909-781-7332
Fax: 909-781-0178

October 29, 2001

To: Snyder & Associates
1054 31st Street, N.W.
Suite 400
Washington, DC 20007

Attn: Ron Snyder

Re: Tag Chip Patent Information

Dear Ron,

The following shall contain NOVA-002 Tag Chip Patent Information.

If you should have any questions regarding this request, please contact our office for further assistance.

Sincerely,

Cari Winant

Cari Winant
Office Administrator

AWARD/CONTRACT

PAGE 1 OF 67

1 CONTRACT (Proc Inst Ident) NO	2 EFFECTIVE DATE	3 REQUISITION/PURCHASE REQ/PROJ	4 THIS CONTRACT IS A RATED ORDER UNDER DPAS (15 CFR 350)
DAAE30-97-C-0012	31 OCT 1996		N (If "9" SEE SEC G)

5 ISSUED BY	CODE	6 ADMINISTERED BY (If other than Block 5)	CODE	7 FOB
DEPARTMENT OF ARMY U. S. ARMY ARDEC PICATINNY ARSENAL, NJ 07806-5000 T. JENSEN SEG AMSTA-AR-PCW-B 201-724-4196	W15QKN	DCMAO SANTA ANA 34 CIVIC CENTER PLAZA P. O. BOX C-12700 SANTA ANA,, CA 92712-2700 (714) 836-2700 Ext. 602	S0513A	D FOB SOURCE = S FOB DESTINATION = D FOB INTERMED = O OTHER = L (SEE SECT E)

8 CONTRACTOR NAME AND ADDRESS (No., Street, city, county, state, and ZIP Code)	CODE	FACILITY CODE	9 TYPE CONTRACT	9a SECURITY CLASS
NOVA R&D, INC. 1525 THIRD STREET SUITE C RIVERSIDE, CA 92507	0P9U3	If "9" for multiple facilities, see Sec. G	J	U

10 DISCOUNT FOR PROMPT PYMT.

1ST	%	DAYS	NET	30
2ND	%	DAYS	OTHER	
3RD	%	DAYS	IF "9" SEE SECT G	

11. SUBMIT INVOICES (4 Copies unless otherwise specified) TO ADDRESS SHOWN IN BLOCK 14	12. SHIP TO/MARK FOR (SEE FORM 69H/966)

13. AUTHORITY FOR USING OTHER THAN FULL AND OPEN COMPETITION:		14. PAYMENT WILL BE MADE BY	CODE
☐ 10 USC 2304(c)		DFAS-COLUMBUS CENTER DFAS-CO-WT/SANTA ANA P.O. BOX 182381 COLUMBUS, OH 43218-2381	SC1006
☐ 41 USC 253(c)			If "9" for multiple disbursing offices, see Sec. G.

15. SEE FORM 69E/69S FOR ITEM NO(s) SCHEDULE OF SUPPLIES/SERVICES, QTY UNIT, UNIT PRICE AND AMOUNT.

16. ACCOUNTING AND APPROPRIATION DATA (SEE FORM 69K)

FAST PAY	KIND CONT	TYPE CONT	ABSTRACT RECIP ADF POINT	SPL CONTR PROVISIONS	DATE SIGNED	SVC/AGENCY USE ONLY	17. SURV CRIT DES	18. TOTAL AMOUNT OF CONTRACT
☐	6	B	SC1006		31 OCT 1996	43FB	C	$ 99,937.39

18. TABLE OF CONTENTS

SEC	DESCRIPTION	PAGE	SEC	DESCRIPTION	PAGE
	PART I - THE SCHEDULE			PART II - CONTRACT CLAUSES	
A	SOLICITATION/CONTRACT FORM	1-4	I	CONTRACT CLAUSES	12-14
B	SUPPLIES OR SERVICES AND PRICES/COSTS	5		PART III-LIST OF DOCUMENTS, EXHIBITS, OTHER ATTACH	
C	DESCRIPTION/SPECS/WORK STATEMENT	6	J	LIST OF ATTACHMENTS	15
D	PACKAGING AND MARKING			PART IV-REPRESENTATIONS & INSTRUCTIONS	
E	INSPECTION AND ACCEPTANCE	7	K	REPRESENTATIONS, CERTIFICATIONS, AND OTHER STATEMENTS OF OFFERORS	16-23
F	DELIVERIES OR PERFORMANCE	8			
G	CONTRACT ADMINISTRATIVE DATA	9	L	INSTRS, CONDS, AND NOTICES TO OFFER.	
H	SPECIAL CONTRACT REQUIREMENTS	10-11	M	EVALUATION FACTORS FOR AWARD	

CONTRACTING OFFICER WILL COMPLETE ITEM 20 OR 21 AS APPLICABLE

20. ☒ CONTRACTOR'S NEGOTIATED AGREEMENT (Contractor is required to sign this document and return 2 copies to issuing office.) Contractor agrees to furnish and deliver all items or perform all the services set forth or otherwise identified above and on any continuation sheets for the consideration stated herein. The rights and obligations of the parties to this contract shall be subject to and governed by the following documents: (a) this award contract, (b) the solicitation, if any, and (c) such provisions, representations, certifications, and specifications, as are attached or incorporated by reference herein. (Attachments are listed herein.)

21. ☐ AWARD (Contractor is not required to sign this document) on Solicitation Number _____, including the additions or changes made by you which additions or changes are set forth in full above, is hereby accepted as to the items listed above and on any continuation sheets. This award consummates the contract which consists of the following documents: (a) the Government's Solicitation and your offer, and (b) this award/contract. No further contractual document is necessary.

22. NAME OF CONTRACTOR	23. UNITED STATES OF AMERICA
BY _____ (Signature of person authorized to sign)	BY _____ (Signature of Contracting Officer)

24. NAME AND TITLE OF SIGNER (Type or print)	25. DATE SIGNED	26. NAME OF CONTRACTING OFFICER (Type or print)	27. DATE SIGNED
Sezen H. Tumer, President	10/31/1996	Paul Milenkowic	31OCT96

STD FORM 26/SDA 67X-E (APR 65)

FORM 69K (REV 10-83)	CONTINUATION SHEET	PROC INSTR IDENT NO DAAE30-97-C-0012	MOD/ORDER NO	PAGE 3	OF 67

PART I SECTION G
ACCOUNTING CLASSIFICATION DATA

ACCTG CLASS REF	APPROPRIATION	LIMIT SUBHEAD	SUPPLEMENTAL ACCOUNTING CLASSIFICATION
AA	21 72040	0000	76D6D03665502.2581 S28017

NON-CLIN/ELIN PAYMENT PROV	CPN RECIPIENT DOAAD	OBLIGATED AMOUNT *	SVC/AGENCY USE ONLY
		99,937.39	665502M4055

DESCRIPTIVE DATA:
C.O. 1A327F6QA11A
PROJECT NO: 7F6QT1

ACCTG CLASS REF	APPROPRIATION	LIMIT SUBHEAD	SUPPLEMENTAL ACCOUNTING CLASSIFICATION

NON-CLIN/ELIN PAYMENT PROV	CPN RECIPIENT DOAAD	OBLIGATED AMOUNT *	SVC/AGENCY USE ONLY

DESCRIPTIVE DATA:

ACCTG CLASS REF	APPROPRIATION	LIMIT SUBHEAD	SUPPLEMENTAL ACCOUNTING CLASSIFICATION

NON-CLIN/ELIN PAYMENT PROV	CPN RECIPIENT DOAAD	OBLIGATED AMOUNT *	SVC/AGENCY USE ONLY

DESCRIPTIVE DATA:

ACCTG CLASS REF	APPROPRIATION	LIMIT SUBHEAD	SUPPLEMENTAL ACCOUNTING CLASSIFICATION

NON-CLIN/ELIN PAYMENT PROV	CPN RECIPIENT DOAAD	OBLIGATED AMOUNT *	SVC/AGENCY USE ONLY

DESCRIPTIVE DATA:

ACCTG CLASS REF	APPROPRIATION	LIMIT SUBHEAD	SUPPLEMENTAL ACCOUNTING CLASSIFICATION

NON-CLIN/ELIN PAYMENT PROV	CPN RECIPIENT DOAAD	OBLIGATED AMOUNT *	SVC/AGENCY USE ONLY

DESCRIPTIVE DATA:

ACCTG CLASS REF	APPROPRIATION	LIMIT SUBHEAD	SUPPLEMENTAL ACCOUNTING CLASSIFICATION

NON-CLIN/ELIN PAYMENT PROV	CPN RECIPIENT DOAAD	OBLIGATED AMOUNT *	SVC/AGENCY USE ONLY

DESCRIPTIVE DATA:

*REPRESENTS NET AMOUNT OF INCREASE/DECREASE WHEN MODIFYING AN EXISTING AC[illegible]

PART I - THE SCHEDULE
SECTION B - SUPPLIES OR SERVICES AND PRICES/COSTS

B-1. LINE ITEM DESCRIPTION: In accordance with this contract, the contractor, independently and not as an agent of the Government, shall provide all necessary materials, labor, equipment, and facilities, except as specified herein to be furnished by the Government, and shall do all that which is necessary or incident to the satisfactory and timely performance of the following Contract Line Item Number (CLIN):

CLIN	SUPPLIES OR SERVICES	QUANTITY	UNIT	AMOUNT
0001AA	Work as set forth in Nova R&D Inc. Small Business Innovation Research Program Proposal, dated 7/3/96, titledA Practical System for a Low Cost Smart Tag & Applicator, Attachment 4.	959	DPPH* @ $104.21	$99,937.39
0001AB	Data (Final Report) in accordance with Section C	1	Lot	Not Separately Priced
			TOTAL	$99,937.39

B-2. FIRM-FIXED-PRICE, LEVEL OF EFFORT TERM:

a. In the performance of CLIN 0001AA of this contract, the contractor shall provide the following level of effort within the time period as set forth in Section F-1 hereof:

*DIRECT PRODUCTIVE PERSON HOURS LEVEL OF EFFORT	COMPOSITE RATE PER HOUR	TOTAL
959	$104.21	$99,937.39

b. DPPH are defined as prime contractor, subcontractor, and consultant actual direct labor hours exclusive of vacation, holiday, sick leave, and other absences.

c. In accordance with FAR 16.207-2, entitlement to full payment is based on the determination by the Government that the required level of effort and reports have been provided and are acceptable.

Part I - The Schedule
SECTION E - INSPECTION AND ACCEPTANCE

E-1. CLAUSE INCORPORATED BY REFERENCE (JUN 1988) (FAR 52.252-2): This contract incorporates one or more clauses by reference, with the same force and effect as if it were given in full text. Upon request, the Contracting Officer will make its full text available.

FEDERAL ACQUISITION REGULATION (48 CFR CHAPTER 1) CLAUSE

CLAUSE NUMBER	FAR CITATION	CLAUSE TITLE	DATE
1	52.246-9	**INSPECTION OF RESEARCH AND DEVELOPMENT (SHORT FORM)**	**APR 84**

E.2 ACCEPTANCE

[ ] Acceptance will be at the Contractor's plant.

[x] Acceptance will be at destination.

E.3 GOVERNMENT PROCUREMENT QUALITY ASSURANCE ACTIONS

Government Procurement Quality Assurance (PQA) actions will be accomplished by the Governments authorized Quality Assurance Representative (QAR) at:

[ ] Contractors Plant

[x] Destination

[ ] Other: The Contractor's plant except for tests conducted at a Government Facility or Proving Ground

Part I - The Schedule
SECTION G - CONTRACT ADMINISTRATION DATA

G-1. INVOICING AND VOUCHERING:

a. Progress Payments: The contractor may submit public vouchers (Standard Form 1034, SEE ATTACMENT 5), not more frequently than monthly, based on the level of effort expended under this contract. The vouchers shall be computed based on the hours of labor performed times the composite rate per hour specified in Section B-2 of this contract.

b. Submit vouchers to: Public vouchers, together with any necessary supporting documentation, shall be submitted to the contract administration office specified in block 6 of page 1, SF-26. (After verification, payment will be made by the paying office shown in block 14).

c. In addition to the hours of labor performed, the contractor shall identify on each public voucher: (1) the contract number, (2) PRON Number. (**Sample ATTACHMENT 5).**

d. Final Report/Payment: At the end of the performance period the contractor will submit a completed DD250 Material Inspection and Receiving Report (**See attachment 6**) with the Final Report submission requirements as stated in Section C.

G-2. CONTRACT ADMINISTRATION: Administration of this contract will be performed by the cognizant office as shown in Block 6, Page 1, Section A, of Standard Form 26. No changes, deviations, or waivers shall be effective without a modification of the contract executed by the Contracting Officer or his or her duly authorized representative authorizing such changes, deviations, or waivers.

G-3. CONTRACTING ACTIVITY REPRESENTATIVES:

	Contractual Matters	Technical Matters
NAME:	Timothy R. Jensen	Dr. Paul Willson
OFFICE CODE:	AMSTA-AR-PCW-B	AMSTA-AR-QAT-T
TELEPHONE NUMBERS:		
COMMERCIAL:	(201)-724-4196	(201)-724-2135
(DSN):	880-4196	880-2135

G-4. IDENTIFICATION OF CORRESPONDENCE: All correspondence and data submitted by the contractor under this contract shall reference the contract number.

G.5 PAYMENT/REMIT-TO ADDRESS
Payment shall be made to the remit-to address shown on the invoice as authorized by the contractor.

G.6 Acceptance of Data
No Government employee is authorized to accept any data with restrictive or proprietary markings without the approval of the Procuring Contracting Officer.

H.3 CALIFORNIA SALES AND USE TAX (AMCCOM # 52.229-4500)(AL 92-1)

If this contract contains either the clause FAR 52.245-2, Government Property (Fixed Price Contracts), or 52.245-5, Government Property (Cost-Reimbursement, Time and Material, or Labor Hour Contracts), California sales tax on the purchase of any tangible personal property for the performance of this contract is not an allowable cost. Such purchases can be made tax-free by giving California vendors resale certificates, the form for which is prescribed by California tax authorities. This California sales tax exemption does not apply to the purchase of any property to be incorporated into real property located in California.

H-4. KEY PERSONNEL: Key personnel (e.g., Principal Investigator, Principal Engineer, or equivalent) must be employed with the firm at the time of award and shall be maintained, to the maximum extent possible, throughout this program. The Principal Investigator must spend more than one-half of his/her time with the firm. Should changes be necessary, the contractor shall notify the Government in writing of the proposed substitutes and their qualifications. Implementation of the changes shall be subject to Government approval.

H-5. METRIC AND PRODUCT ASSURANCE REQUIREMENTS: The contractor shall assure that all deliverables under this contract shall meet industry standards of quality and, where practical, metric measurements.

H-6. SAFETY HAZARDS: The contractor shall identify, control, and document the hazards associated with this effort and the control methods necessary to eliminate or control the hazards. Significant items shall be addressed in status meetings and included in the final report.

H-7. ENVIRONMENTAL: The contractor agrees to the following:

a. All activities performed under this contract shall be conducted in accordance with Federal, State, and local environmental laws and regulations.

b. Any facility to be used in the performance of this contract shall be in compliance with all Federal, State, and local environmental laws and regulations for its intended use.

H-10. 252.201-7000 CONTRACTING OFFICER'S REPRESENTATIVE. (DEC 1991)

(a) "Definition. Contracting officer's representative" means an individual designated in accordance with subsection 201.602-2 of the Defense Federal Acquisition Regulation Supplement and authorized in writing by the contracting officer to perform specific technical or administrative functions.
(b) If the Contracting Officer designates a contracting officer's representative (COR), the Contractor will receive a copy of the written designation. It will specify the extent of the COR's authority to act on behalf of the contracting officer. The COR is not authorized to make any commitments or changes that will affect price, quality, quantity, delivery, or any other term or condition of the contract.

CLAUSE NUMBER	FAR CITATION	CLAUSE TITLE	DATE
17.	52.232-28	ELECTRONIC FUNDS TRANSFER PAYMENT METHODS	APR 1989
18.	52.233-1	DISPUTES	MAR 1994
19.	52.233-3	PROTEST AFTER AWARD	AUG 1989
20.	52.245-18	SPECIAL TEST EQUIPMENT	FEB 1993
21.	52.246-16	RESPONSIBILITY FOR SUPPLIES	APR 1984
22.	52.249-1	TERMINATION FOR CONVENIENCE OF THE GOVERNMENT (FIXED PRICE) (SHORT FORM)	APR 1984
23.	52.253-1	COMPUTER GENERATED FORMS	JAN 1991

II. DOD FAR SUPPLEMENT (48 CFR CHAPTER 2) CLAUSES

CLAUSE NUMBER	DFARS CITATION	CLAUSE TITLE	DATE
1.	252.204-7000	DISCLOSURE OF INFORMATION	DEC 1991
2.	252.204-7003	CONTROL OF GOVERNMENT PERSONNEL WORK PRODUCT	APR 1992
3.	252.225-7031	SECONDARY ARABBOYCOTT OF ISRAEL	JUN 1992
4.	252.227-7016	RIGHTS IN BID OR PROPOSAL INFORMATION	JUN 1995
5.	252.227-7017	IDENTIFICATION AND ASSERTION OF USE, RELEASE,OR DISCLOSURE RESTRICTIONS	JUN 1995
6.	252.227-7018	RIGHTS IN NONCOMMERCIAL TECHNICAL DATA AND COMPUTER SOFTWARE--SMALL BUSINESS INNOVATIVE RESEARCH (SBIR) PROGRAM	JUN 1995
7.	252.227-7019	VALIDATION OF ASSERTED RESTRICTIONS--COMPUTER SOFTWARD	JUN 1995
8.	252.227-7030	TECHNICAL DATA--WITHHOLDING OF PAYMENT	OCT 1988
9.	252.227-7034	PATENTS--SUBCONTRACTS	APR 1984
10.	252.227-7036	CERTIFICATION OF TECHNICAL DATA CONFORMITY	MAY 1987
11.	252.227-7037	VALIDATION OF RESTRICTIVE MARKINGS ON TECHNICAL DATA	JUN 1995

PART III - LIST OF DOCUMENTS, EXHIBITS, AND OTHER ATTACHMENTS
SECTION J - LIST OF ATTACHMENTS

J.1 LIST OF DOCUMENTS, EXHIBITS, AND OTHER ATTACHMENTS

Attachment 1	Disclosure of Lobbying Activities (form)
Attachment 2	Clear Technical Information for Public Release (form)
Attachment 3	SBIR Program Instructions for submitting Phase II Proposals
Attachment 4	Copy of Contractor's Proposal
Attachment 5	Example of Public Voucher for Progress Payments and Final Payment
Attachment 6	DD Form 250 Material Inspection and Receiving Report

DISCLOSURE OF LOBBYING ACTIVITIES

Approved by OMB 0348-0046

Complete this form to disclose lobbying activities pursuant to 31 U.S.C. 1352
(See reverse for public burden disclosure.)

1. Type of Federal Action:	2. Status of Federal Action:	3. Report Type:
☐ a. contract b. grant c. cooperative agreement d. loan e. loan guarantee f. loan insurance	☐ a. bid/offer/application b. initial award c. post-award	☐ a. initial filing b. material change For Material Change Only: year _____ quarter _____ date of last report _____

4. Name and Address of Reporting Entity:	5. If Reporting Entity in No. 4 is Subawardee, Enter Name and Address of Prime:
☐ Prime ☐ Subawardee Tier _____, *if known:* Congressional District, *if known:*	Congressional District, *if known:*
6. Federal Department/Agency:	**7. Federal Program Name/Description:** CFDA Number, *if applicable:* _____
8. Federal Action Number, *if known:*	**9. Award Amount, *if known:*** $
10. a. Name and Address of Lobbying Entity *(if individual, last name, first name, MI):*	**b. Individuals Performing Services** *(including address if different from No. 10a)* *(last name, first name, MI):*

(attach Continuation Sheet(s) SF-LLL-A, if necessary)

11. Amount of Payment *(check all that apply):*	13. Type of Payment *(check all that apply):*
$ _____ ☐ actual ☐ planned	☐ a. retainer ☐ b. one-time fee ☐ c. commission ☐ d. contingent fee ☐ e. deferred ☐ f. other; specify: _____
12. Form of Payment *(check all that apply):* ☐ a. cash ☐ b. in-kind; specify: nature _____ value _____	

14. Brief Description of Services Performed or to be Performed and Date(s) of Service, including officer(s), employee(s), or Member(s) contacted, for Payment Indicated in Item 11:

(attach Continuation Sheet(s) SF-LLL-A, if necessary)

15. Continuation Sheet(s) SF-LLL-A attached: ☐ Yes ☐ No

16. Information requested through this form is authorized by title 31 U.S.C. section 1352. This disclosure of lobbying activities is a material representation of fact upon which reliance was placed by the tier above when this transaction was made or entered into. This disclosure is required pursuant to 31 U.S.C. 1352. This information will be reported to the Congress semi-annually and will be available for public inspection. Any person who fails to file the required disclosure shall be subject to a civil penalty of not less than $10,000 and not more than $100,000 for each such failure.

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You can submit only one copy of the videotape and script, but it will slow down the approval process. At least 60 days lead time is preferred.

For further information on this process, contact either your firm's contracting officer or the Picatinny public affairs office at (201) 724-6365.

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(Use this space, and additional pages as necessary, to make additional remarks or written changes to the submitted material. If changes are made directly on the material, a note to that effect in the *Required Approvals* section under "Remarks" is all that's necessary.)

Note that this side of the form is only used for comments and instructions

43003

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PLACE: DATE(S): DoD Sponsored: ❑ Yes ❑ No

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See reverse for instructions

ATTACHMENT 3

Cover all items listed in Section 4 of these instructions in the order given. The space allocated to each will depend on the problem chosen and the principal investigator's approach. The proposal should address the potential commercial applications or Government use of the research or research and development.

4. PROPOSAL FORMAT

a. **Cover Sheet.** Complete Appendix A as page 1 of your proposal. Copies of Appendices will be provided by the Army to all Phase I winners at the time of Phase I contract award.

b. **Project Summary.** Complete the Project Summary, Appendix B, as page 2 of your proposal. Include a brief description of the problem or opportunity, project objectives, description of the effort and anticipated results. Expected benefits and Government or private sector applications of the proposed research should also be summarized in the space provided. The Project Summary of successful proposals will be submitted for publication with unlimited distribution and, therefore, will not contain classified or proprietary information.

c. **Results of the Phase I Work.** Discuss the objectives of your Phase I effort, the research conducted, findings or results, and estimates of technical feasibility. As stated in the original solicitation, if you have not completed your Phase I effort, language used to report Phase I progress in a Phase II proposal may be used verbatim in the Phase I final report with changes to accommodate results after Phase II proposal submission and modifications required to integrate the final report into a self-contained, comprehensive and logically structured document.

d. **Phase II Technical Objectives and Approach.** List the specific technical objectives of the Phase II research and describe the technical approach to be used in meeting these objectives. Methods designed to achieve each objective should be discussed explicitly and in detail.

e. **Phase II Work Plan.** Provide an explicit, detailed description of the Phase II approach. The plan should indicate what is planned, how and where the work will be carried out, a schedule of major events, and the final product to be delivered. A Phase II effort should attempt to accomplish the technical feasibility demonstrated in Phase I, including any potential transition of results to the Government or private sector. This section should be a substantial portion of the total proposal and must clearly show an advancement in the research, or research and development, appropriate for Phase II.

facilities where the proposed work will be performed meet environmental laws and regulations of federal, state (name) and local governments for, but not limited to, the following groupings: airborne emissions, waterborne effluents, external radiation levels, outdoor noise, solid and bulk waste disposal practices, and handling and storage of toxic and hazardous materials.

k. **Consultants.** Involvement of university, academic institution, or other consultants in the project may be appropriate. If such involvement is intended, it should be described in detail and identified in the cost proposal. As stated previously, a minimum of one-half of the research or research and development effort must be performed by the firm proposing Phase II.

l. **Prior, Current and Pending Support.** If a submitted proposal is substantially the same as another proposal that has been funded, is now being funded, or is pending with another Federal agency or DoD Component or the same DoD Component, the proposer must indicate the action on Appendix A and provide the following information:

(1) The name and address of the agency(s) or DoD Component to which a proposal was submitted, will be submitted, or from which an award is expected or has been received.

(2) Date of proposal submission or date of award.

(3) Title of proposal.

(4) Name and title of principal investigator for each proposal submitted or award received.

(5) Title, number, and date of solicitation(s) under which the proposal was submitted, will be submitted, or under which award is expected or has been received.

(6) If award was received, state contract number and the sponsoring agency.

(7) Specify the applicable topics for each SBIR proposal submitted or award received.

NOTE: If this section does not apply, state in the proposal ***"No prior, current, or pending support for proposed work."***

a Company Commercialization Report regardless of the number of Phase II awards received. This report will list the name of the awarding agency, date of award, contract number, topic or subtopic, title, and award amount for each SBIR Phase I and Phase II project performed by the company. In addition, a description of the commercialization status of each Phase II project is required (This required proposal information will count toward the page limitation for the proposal).

o. Bindings. Do not use special bindings or covers. Staple the pages in the upper left hand corner of each proposal.

c. **Evaluation Criteria (Phase I Awards Under DoD SBIR Program Solicitation 93.2 and Subsequent Solicitations).** All proposals will be reviewed for overall merit based on the evaluation criteria the DoD SBIR Program Solicitation and repeated below:

(1) The soundness and technical merit of the proposed approach and its incremental progress toward topic or subtopic solution.

(2) The potential for commercial (Government or private sector) application and the benefits expected to accrue from this commercialization.

(3) The adequacy of the proposed effort for the fulfillment of requirements of the research topics.

(4) The qualifications of the proposed principal/key investigators, supporting staff and consultants.

All criteria will be weighted equally. Qualifications include not only the ability to perform the research and development but also the ability to commercialize the results. A proposal's commercial potential will be evaluated using the criteria in the DoD SBIR Program Solicitation and repeated below:

(1) The small business concern's record of commercializing SBIR of other research.

(2) The existence of second phase funding commitments from private sector or non-SBIR funding sources.

(3) The existence of third phase follow-on commitments for the subject of the research.

(4) The presence of other indicators of commercial potential of the idea.

Phase II proposals will be subject to a detailed technical evaluation by technology experts and by a panel of senior Army technologists. The evaluation may include on-site evaluations of Phase I efforts by government personnel. Final decisions will be made by a senior Army committee based upon the panel's recommendations in light of the scientific and technical evaluations and other factors, including a commitment for co-funding or follow-on funding, the possible duplication with other research or research and development, program balance.

b. **Reports.** For incrementally funded Phase II projects, an interim, midterm written report is required 30 days prior to the conclusion of the first incrementally funded period. Phase II projects funded for the entire contract period will submit a written interim, midterm report 30 days prior to the conclusion of the first year of performance. Two copies of the interim report for the Phase II work must be submitted to the sponsoring agency and AMXRO-W-SBIR (two copies each). A two page executive summary shall be submitted with the interim reports. The executive summary will identify, to date, the purpose of the work, a brief description of the work carried out, any findings or results, and potential applications of the effort. The summary may be published by DoD and, therefore, must not contain proprietary or classified information. The balance of the interim report should discuss, in detail, the project objectives, work carried out, and results obtained, thus far. The government reserves the right to terminate a contractor, after one year of performance, if the contractor fails to perform the work contracted or budgetary constraints prevent second year funding.

Six copies of a final report on the Phase II work must be submitted in accordance with the negotiated delivery schedule. The final report will be submitted within thirty days after completion of the Phase II effort. The final report shall include a single page project summary as the first page identifying the purpose of the work, a brief description of the work carried out, the findings or results, and potential applications of the effort. The summary may be published by DoD and, therefore, must not contain proprietary or classified information. The balance of the report should indicate, in detail, the project objectives, work carried out, and results obtained.

e. **Payment Schedule.** Per DoD SBIR Program Solicitation.

f. **Markings of Proprietary or Classified Proposal Information.** Per DoD SBIR Program Solicitation.

g. **Copyrights, Patents and Technical Data Rights.** Per DoD SBIR Program Solicitation.

h. **Joint Ventures or Limited Partnerships.** Per DoD SBIR Program Solicitation.

i. **Contractor Commitments.** The information in the DoD SBIR Program Solicitation is applicable to the types of provisions that may be included in a Phase II contract.

ATTACHMENT 4

U.S. DEPARTMENT OF DEFENSE

SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM

PROPOSAL COVER SHEET

Failure to fill in all appropriate spaces may cause your proposal to be disqualified

TOPIC NUMBER: A96-009

PROPOSAL TITLE: A Practical System for a Low Cost Smart Tag and Applicator

FIRM NAME: NOVA R&D, Inc.

PHASE I or II PROPOSAL: 1

Technical Abstract (Limit your abstract to 200 words with no classified or proprietary information/data.)

A feasibility study is proposed for developing a practical low cost smart tag and a remote programmer/reader system using a radio frequency link. The required information will be stored in the tag's non-volitile memory. The information can be written and read out as many times as needed.

A novel applicator for the smart tag is also proposed. The applicator will be simple in design. It will apply the smart tag onto any type of package, box, bag, luggage, and crate of various thickness and stiffness while they are transported on a conveyer. The tag will be applied to the item as it is moving with arbitrary order, shape, size, orientation, and position. The conveyor can reach maximum speed of two hundred feet per minute. The material covering the item can be cloth, metal, plastic, paper or wood.

During Phase I, the feasibility of the smart tag and the applicator will be experimentally demonstrated. During Phase II, prototypes of the smart tag, the remote programmer/reader system and the versatile applicator will be fabricated. In Phase III, smart tag, remote programmer/reader system and the tag applicator will be commercialized.

Anticipated Benefits/Potential Commercial Applications of the Research or Development.

The results of the Phase I and II programs will be a practical low cost smart tag, a remot programmer/reader system and a novel versatile applicator. The smart tags and the applicator can be used for tagging any type of conveyor transported item. It can also be used in many other applications where automatic tagging is required.

List a maximum of 8 Key Words that describe the Project.

Tags	Smart Tags
Remotely programmable tags	Tag applicator

achieve low resistivity. The skin depth is the distance the microwave currents penetrate into the surface of the metal layer. It is within this characteristic depth that the electromagnetic field propagates. This skin depth varies with the frequency and dielectric constant of the surrounding media. Careful attention will be paid during modeling and simulations, to the wave nature of the interaction to achieve optimum design. (Very short radio waves or microwaves will be used for this project to achieve higher efficiency.)

The external remote programmer/reader will send out radio frequency power to the antenna on the chip. The received power will be used to charge up a capacitor. The output of the capacitor will then be used to power the chip. The rest of the circuit on the chip will be low power CMOS circuits that will receive the signal from the remote programmer/reader and store the information onto the non volatile EEPROM memory. If a read request comes from the programmer/reader the chip will also have the functionality to transmit the contents of the memory through the antenna.

Other functions such as having a unique tag number for identification of which tag is programmed or read out will also be studied and implemented if required. Such a unique identification number can be important if there is more than one tag inside the aperture field of the remote programmer/reader.

The cost of the chip will be kept as low as possible by using small die size on large 6" or 8" wafers. For example, from a single 8" wafer we expect to get approximately 30,000 1 x 1 mm, 10,000 2 x 2 mm and 3,000 3 x 3 mm dies. Small dies with relatively simple circuitry may have exceptionally high yield reaching up to 80%. In large quantities each wafer is expected to cost much less than $400 to process. This shows that even with 50% yield at $400 per wafer the fabrication cost of the tags is in cents. The cost of initial prototypes will be much higher due to the low numbers required and the large non-recurring engineering cost which includes the mask set.

A second factor involved in the cost is the selection of the working tags for deployment. Since the production tags will be completely self contained the testing will not require a probe card and a costly probe station. The dies can pass in front of a test and selection system placed on to a tiny conveyer belt. The test system will be very similar in design to the remote programmer/reader unit. It will be programmed to power the tag, write and read several coded data to test and select the working chips. It may also program a unique ID number on to the tag if required. Such a system can be built at NOVA during Phase III.

In summary, the remote programmer/reader will produce radio waves tuned to the tag antenna for transferring power to the chip. It will also transmit the data to the tag with or without an identification number. The identification number can be already programmed into the tag before application. It will also have the capability to ask the chip to send its memory contents and be able to read the data transmitted by the tag. Each cycle; send power, program tag, request data from tag and read tag, will be done sequentially. These and other possible functionality and circuit ideas will be studied during Phase I.

A. 3. Proposed Applicator Concept

The requirements for the applicator is extensive as described in **Section A1**. It is proposed a simple but novel technique to meet these requirements. The proposed applicator will be made of a simple glue gun. A jelly type of glue that does not harden but retains its stick quality for a long period of time measured in days will be used. The tags will be embedded into the glue and glue balls containing a tag will be propelled onto a baggage. The diameter of the glue ball will be between 3 to 5 mm. The glue will be the kind used for temporary attachment of paper, wood, plastic, metal or any kind of material to each other. Only problematic surfaces may be oily surface and possibly teflon. This type of glue practically attaches itself to any known material. The most effective glue will be selected during Phase I.

The selected glue can be transparent or may be used in different colors. A transparent glue can match most surfaces and will be the low cost way to proceed. However, it will show the silicon tag inside. If a colored glue is needed to match the color of the item then a color reader will be required such as a simple video camera. The output of the color video camera will be used to select the most appropriate glue color. This will also require several applicators or one applicator with several

B. PHASE I TECHNICAL OBJECTIVES

B. 1. Phase I Tasks

The tasks of proposed Phase I program are given below:

Task 1. Design and simulate the electronic circuits for the proposed smart tag system.

Task 2. Selectively layout the tag circuitry onto silicon with buffered pads at critical locations for testing and evaluating the circuits developed.

Task 3. Investigate different types of glues for use by the proposed tag applicator.

Task 4. Study performance of the selected glues on different baggage and cargo materials.

Task 5. Set up a test system for the prototype tag chips.

Task 6. Fabricate, test and evaluate prototype tag chips.

Task 7. Search for a suitable glue gun, evaluate possible candidates, study the modification of selected devices or if necessary design a custom glue gun.

Task 8. Investigate and prepare a preliminary design of a remote programmer/reader system for the tags.

Task 9. Study the charge transmission and storage on the tag chip.

Task 10. Investigate the capability of the tag circuitry to transmit data back to the remote reader.

Task 11. Present and demonstrate the Phase I results to DOD/Army officials.

Task 12. Write Phase I Final Report.

B. 2. Phase I Task Schedule

Work will start immediately on the design, modeling and simulation of the smart tag electronic circuits especially the antenna system (Task 1). This work is expected to take about 1 month. As soon as the simulations are completed the silicon layout of a prototype chip will begin (Task 2). This will take about 1.5 months to complete.

The investigation of the glue types will start as soon as the tag chip simulation is underway (Task 3). It will take about 1.5 months to complete the initial work. However, search for the best glue will carry on at a much reduced activity level until Phase III in case better products come to market. The performance of the selected glues will be studied (Task 4) for about one month.

A benchtop test system will be designed and developed (Task 5) as soon as the tag electronics is decided. This work is expected to take about 2 months. When the tag chip silicon layout work is completed it will be sent to manufacture using the low cost MOSIS program (Task 6). It will take about 6 weeks to fabricate the prototypes at the foundry. As soon as the chips arrive they will be tested and evaluated (Task 6). The total work is expected to take about 2 months.

A search will be carried out, as soon as a glue is selected, for a suitable glue gun (Task 7). If found the gun may be modified for tag application. If none can be found then a custom glue gun will be designed. This work is expected to take about 3.5 months.

As soon as the tag circuitry is decided the design of the remote programmer/reader will start (Task 8). It is expected to take about 3.5 months to complete. The charge (Task 9) and data transmission (Task 10) to and from the tag chip will be studied as soon as the tag chip testing is completed. These tasks will take about 1.5 months. The prototype tags and the work on the applicator will be presented to DoD/Army officials at the end of the project period (Task 11). The Phase I Final Report will be written during the final month of the project (Task 12).

One of these is the width of the antenna line. It must be carefully optimized as the adjacent layers can be electrically shorted to form a single line. The thickness and width of the antenna line should also be kept as large as possible. Since the aim is also to produce the smallest chip area, a compromise must be made that will work. Three dimensional simulations of the antenna system will be used to accomplish this.

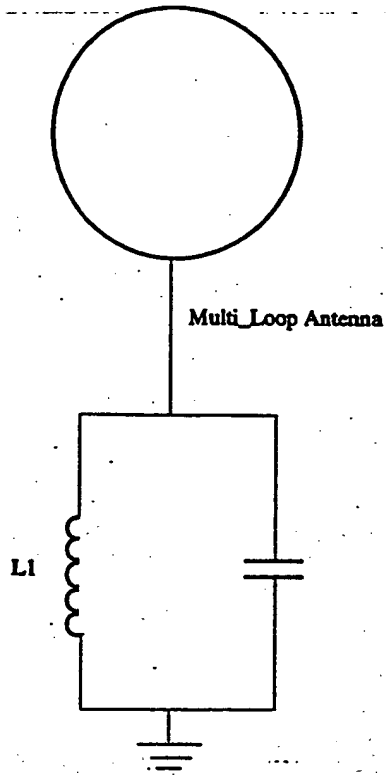

Figure 1. Parallel tuned antenna circuit.

The efficiency of a loop antenna is related to the area as the fourth power and the induced current squared as given in the formula below.

C. 3. Transmitting through a Small Circuit Loop Antenna

The radiated power from a loop antenna can be obtained (Ramo, Whinnery and Van Duzer, 1965) by the integration of the time averaged Poynting vector which is the power density at any point.

$$\bar{P} = \bar{E} \times \bar{H}$$

In the spherical coordinates, the total power radiated is

$$W = \int_0^{\pi} \int_0^{2\pi} P_r r^2 \sin\theta d\theta d\phi = \int_0^{\pi} \int_0^{2\pi} K \sin\theta d\theta d\phi$$

where P_r is the radical component of the Poynting vector and K is defined as the radiation intensity. For a loop antenna, K is obtained as

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10 volts. One micro amp of current could be provided for 10 millisecond from this much stored charge. All the charge will not be provided at 10 volts during this time if a steady current at this value was drawn from the capacitor. The total integrated circuit will be designed to operate using minimal power. Techniques to keep the power usage low are to use split threshold voltages (Vt). A higher threshold voltage will be used on standby current circuits. A lower threshold voltage will be used on dynamic circuit MOSFET's. A lower power is achieved in the digital section if the ratio in transistor sizes is optimized toward power consumption. CMOS inverters typically are designed to center the switch point and equalize the rise and fall times between the N and PMOS devices. But power is minimized by using less gate area, sizing for drive required from each stage, and reducing the cross over conduction during switching. A total average circuit current of 100 nanoamp will be a system goal for operation of the tag circuit. Burst current for transmission will be much higher, but the system interface could recharge the system for a brief time after each transmission.

A two antenna system, where one tuned for receiving power and the other tuned for receiving and transmitting data will be studied and simulated. If such a system is found to be feasible then the chip could be receiving continuous power while receiving and sending data.

C. 5. The Description of the Complete Tag System

The complete tag integrated circuit chip is shown in a system block diagram in **Figure 3.** Each section is shown with a label for its function and the connection to other sections through the data path(s).

Received microwave power is rectified and stored. The rising voltage on the power capacitor will cause the chip to turn on when a sufficient amount of charge is received to activate the system clock and power on reset. After a number of clock cycles the chip is fully charged and a valid read or write signal sent by the remote programmer/reader module is detected by the band pass filters. These filters produce an output which is an analog voltage, if the voltage level is sufficiently high, a power valid signal is sent from the comparators. The read/write flip flop is then latched to reflect the detected state.

The read or write signal is also sent to the chip control section and the memory. The control steps through a set of states reflecting a read or a write cycle. After the read or write cycle the latch is cleared and the chip looks for another read or write signal from the remote programmer/reader.

The reply code is a special section designed to give each chip a unique reply word. This word tells the remote programmer/reader the circuit is ready to be written to or expect to transmit data. The system interface of each chip will be designed to have about one third of a second to interface with the remote programmer/reader. This time is reduced by the time required to power up the chip. Allowing 200 milliseconds for the chip to charge leaves 130 milliseconds for communication.

This 130 milliseconds is the time allotted for the chip to run through its control routine and several read/write cycles. A 100 kHz system clock will complete 13,000 cycles in the allotted time. Careful use of this time and on chip power management by the control section will allow adequate time for several read/write cycles at a conservative rate to verify proper chip information and that the data is correctly stored.

An electrically erasable programmable read only memory (EEPROM) is selected as the most suitable memory for the tag chip. An EEPROM offers non volatile and reprogrammable memory. Different kinds of EEPROMs and other memory circuits will be investigated for application to the proposed tag chip. New ideas will be also investigated and simulated. The circuit which requires the least power to write and read will be selected.

The tag chip will be reprogrammed on activation by the transmission of the write code. A control section will activate an on chip voltage multiplier and boost the write voltage up to the correct voltage when the write mode of operation is received. The memory will be organized as a 10 to 1,000 byte cell depending on the available power for the prototype chips. For production version tags the memory size is expected to be a few thousand bytes. If writing into the memory becomes a

the remote programmer/reader one or both (if the circuit is set to read mode) of the filters will be powered down to reduce power consumption.

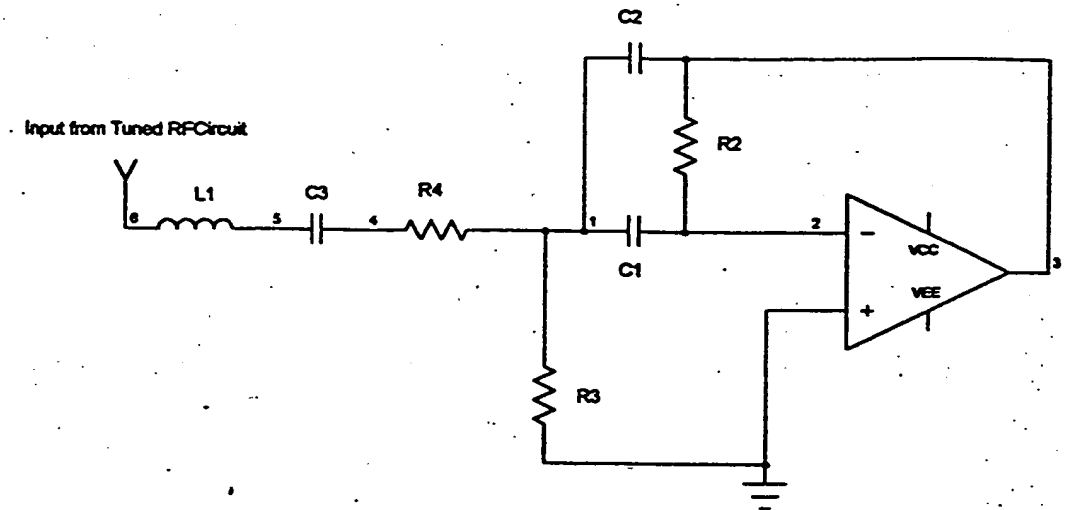

Figure 4. High gain bandpass filter.

The output of the filters will be sent to a CMOS comparator which will latch high or low if the signal level is above the reference level. The output of the comparator will determine the write or read mode for the tag chip. These filters will be an important part of the circuit. They will be fully simulated and optimized. They will be powered up at the end of each write/read cycle to detect the next command.

C. 7. Master System Clock

The master clock for the tag chip will be designed around a simple 3 stage inverter circuit (Figure 5). The operation frequency is determined by the resistors R1, R2, and capacitor C1. The frequency of operation can be set during processing and will vary about 10 to 15 percent depending on the variation of the process parameters. A 1 MHz clock speed could be achieved if the values for R1 and R2 are set to 22 KΩ with C1 adjusted to 9.9 pF. This clock speed is fairly high and less power will be used by the clock circuit if the resistors are set to 200 KΩ. This will reduce the clock speed to the 100 kHz range. Analysis and simulation of the overall system will determine the best frequency to use. Since the system is independent and asynchronous the variation in the operation speed will cause no problem for the read/write system.

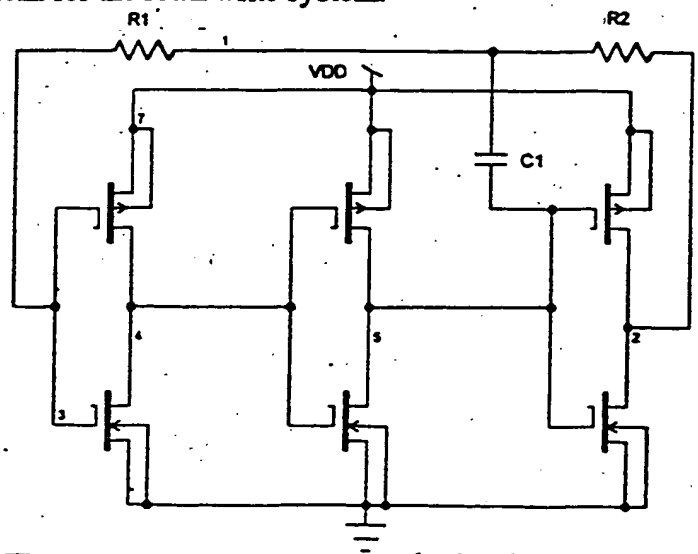

Figure 5. Three stage master system clock circuit schematic diagram.

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Detection of the signal is dependent on the background radiation and the extraneous noise. Careful choice of the reception frequency will be part of the system design to put the center frequency in an interference free wavelength region. The ambient microwave noise background is related to temperature and the bandwidth of the receiver. If the interface receiver is designed for a very narrow bandwidth of 1 MHz, the total thermal noise power is approximately 4 femto watts. Thus the system will have a signal to noise ratio of 50 based upon the small radius antenna of 1 millimeter length. A 1 centimeter antenna will have a signal to noise ratio of 500,000. Therefore, based on these simplified calculations, a system antenna with a loop radius of 3 millimeters will give a signal to noise ratio of 4,000. These theoretical calculations are based on signal power at the emitter or transmitter. Any reduction of power at the receiver will be related to the total angle of transmission, and the distance from the source proportional to the inverse of the distance. Therefore, it will be designed to receive and transmit without any preferential direction, to allow the tag chip to have an arbitrary orientation.

C. 10. Voltage Booster Circuit

Upon reception and verification of a valid write signal, the control section will activate the voltage booster circuit. This circuit is designed to charge a stack of capacitors in series at a low voltage. This series stacking is achieved by means of a combination of capacitors and diodes organized as shown in the voltage booster schematic circuit (**Figure 7**). In action the system clock is used to charge the three capacitors in an alternating fashion to multiply the clock voltage to a voltage high enough to bias the write voltage and inject charge into the floating gate electrodes of the EEPROM array. A one or a zero can be written to a memory cell site by application of the write voltage and the address byte.

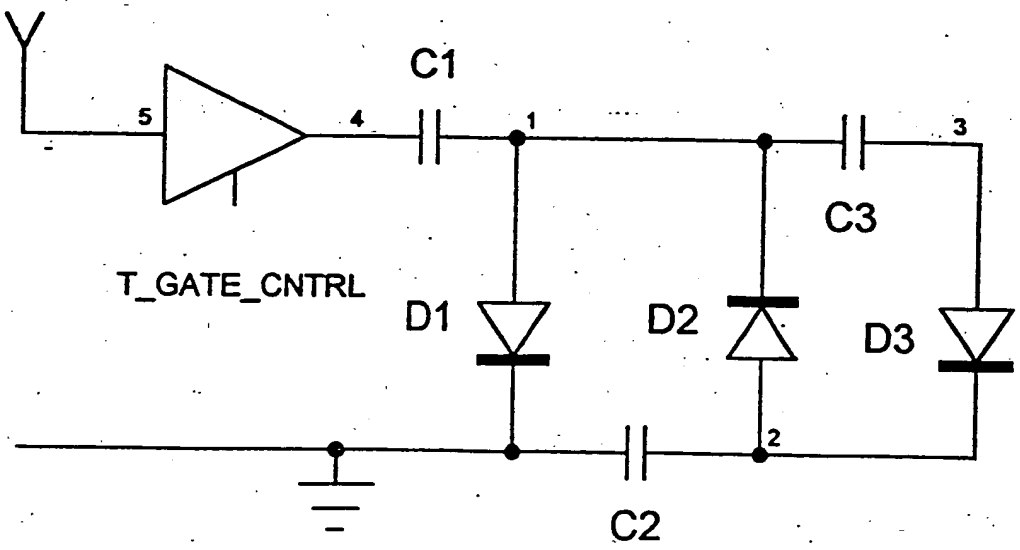

Figure 7. Voltage Booster schematic circuit diagram.

C. 11. CMOS Comparator Circuit

Each bandpass filter provides an analog output depending upon the magnitude of the signal received. In order to have this signal drive digital logic it must be latched to a high or low DC level. This function is accomplished by the CMOS comparator. This circuit is illustrated in **Figure 8**. The input stage is composed of both N and PMOS feedback loops which determines the switching level of the comparator. The circuit achieves this adjustment through varying the MOSFET width to length ratio. These values are determined through computer aided simulation of the circuit operation. This circuit is simple and it is process insensitive. It does not require the use of a separate reference generator. These are all key benefits for the low power requirements of the tag electronics.

The control register continue to switch in and out the control words as the D shift register is incremented. At the end of the register the sequence is started to open the bandpass filters for detection of another control command from the interface system.

C. 13. EEPROM Memory Organization

The EEPROM memory (**Figure 10**) is organized to read and write under the address control. A single cell of a core memory is shown in **Figure 10**. The EEPROM cells are MOSFETS with the extra floating gate controlled by the ROW LINE. In write operation the appropriate column is selected by the column multiplexer. After selection the row line is pulsed to erase all the cells to zero. A one can be written to the appropriate cell by selection of the row select line. The high voltage switch is enabled and a high level signal is applied to the drain of the MOSFET selected for write. The MOSFET stores a one when it is selected. In read operation the cell is addressed by the row and column registers. Each column will be high corresponding to a stored zero and low corresponding to a store one. The sense amplifier and logic creates the correct output sense for positive logic.

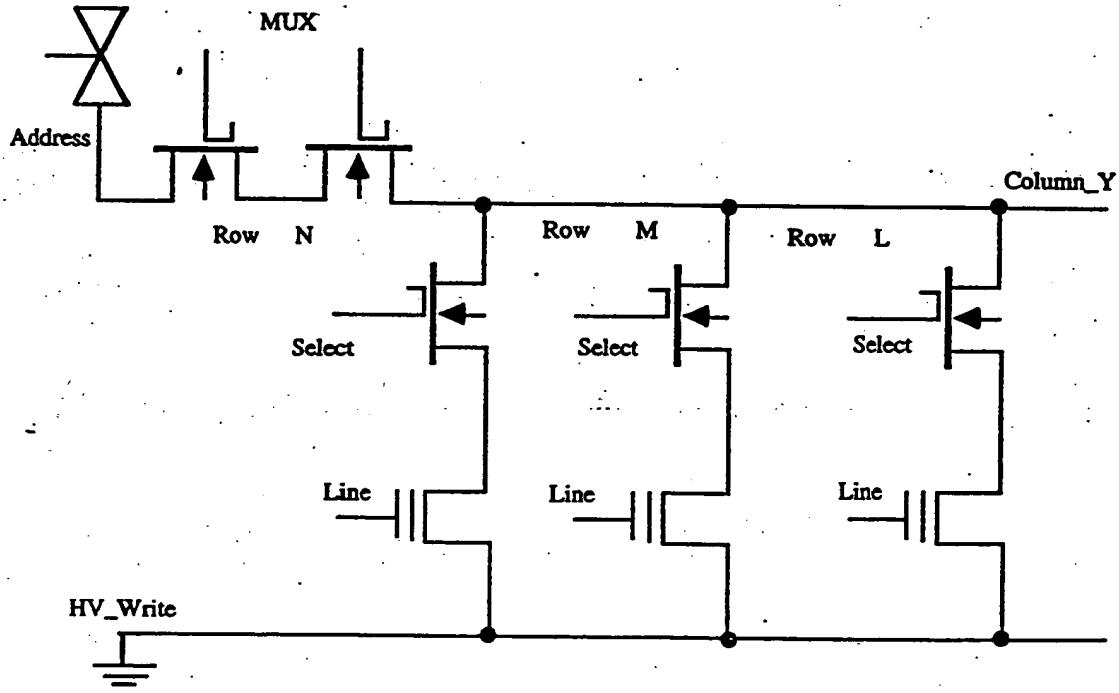

Figure 10. The EEPROM memory circuit (only one cell is shown).

C. 14. Estimated Total Power Dissipation

The total chip power is dependent on the size of the memory, the amount of control logic and the speed of operation. An estimate of the total power dissipation can be calculated using the power per gate and the number of gates (**Table I**). For the tag chip the amount of memory in the prototype Phase I circuit will be smaller than for the Phase II work. We will discuss here the small Phase I prototype chip.

A typical memory cell is composed of six transistors. The number of cells of this type are in the temporary registers used for data load, addressing and control latch. The control logic will be built into a fixed ROM based state machine with virtually no power dissipation. One program routine is reserved for the read operation and the second program routine is designed for the write operation. Therefore, a one or zero of the appropriate register will be placed on the control output bus by sequencing through the control shift register with the system clock. An approximate estimate has

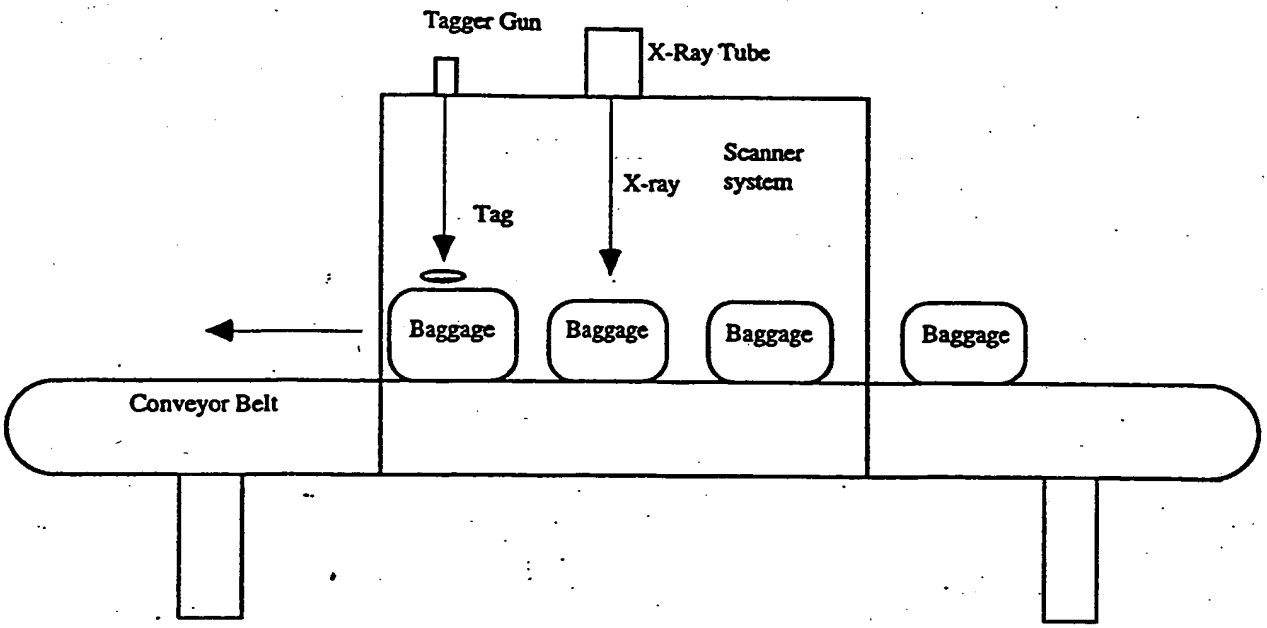

Figure 11. The side view of the x-ray scanner with smart tag applicator.

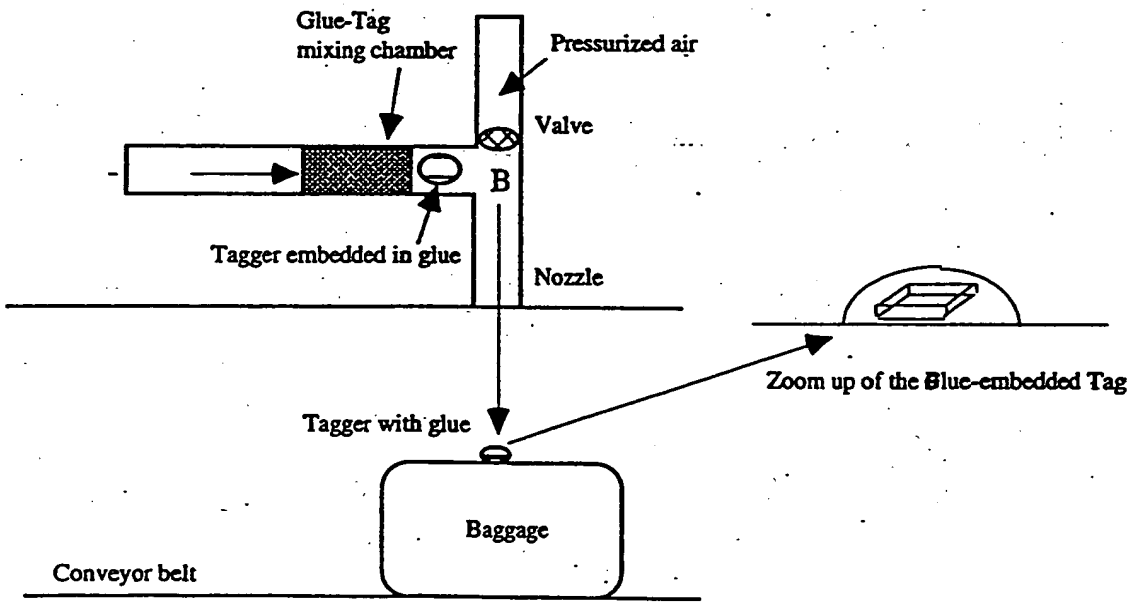

Figure 12. The concept for the applicator mechanism (front view).

The mechanism of transferring the glue-tag combination from the mixing chamber to the area underneath the air valve can be a piston or another mechanism. This will be investigated. As mentioned above the tag chip can be embedded into the glue inside the applicator using a tape conveyor carrying the tag chips at regular intervals similar to those used for transporting surface-mount components. The tag chip is then dislodged from the tape and embedded into the soft glue by the pressure of the glue or using the piston.

The top view of the glue gun concept is shown in **Figure 13**. The LED and the photodiode sensor (**Figure 13**) are used to verify that the glue in chamber A has an embedded tag chip. This

The second project is a nondestructive imaging inspection system for large and dense objects using x rays. Both projects use silicon strip detectors. A derivative of the second project is also started. It is an automatic baggage inspection system for USDA and FAA, a linear pixel CdZnTe pad detector array with 1 mm pitch (active area 4 mm x 32 mm) and a 32 channel fast mixed signal ASIC (FESA) chip for reading out these detectors are being developed. The first prototypes have been fabricated. The ceramic carrier, electronics and test station have been made. The experience gained on the development of the FESA chip will be important for this project.

There are two major medical projects progressing at NOVA. The first project is the high sensitivity single photon emission computed tomography (SPECT) system. The second medical project is a high resolution digital mammography system. Both projects have been funded by NIH. Solid state detectors such as silicon strip, CdZnTe pad and silicon pixel detectors are used in these projects. The design of a prototype pixel detector with its dedicated readout ASIC chip has been developed and tested. This is a charge integration type mixed signal ASIC chip with TDI capability different than the other ASIC chips. We are now designing the second, full scale, version of this chip. This new front-end readout chip will bring new capability to NOVA's solid state detectors. The experience gained on this third ASIC chip will be also important for the proposed project.

Two more proposals were recently funded. They are for a new high sensitivity scintimammography system and a CdZnTe pixel detector based high contrast digital mammography system. All these projects are based on solid sate detectors with custom mixed signal ASIC readout chips.

Also, NOVA has finished the development of a portable hand-held narcotics detector under an SBIR Phase II contract with DOT/Coast Guard. The prototype unit has recently proved its capability by being instrumental in detecting several concealed large narcotic drug shipments. The Phase III marketing of this detector is in progress in cooperation with our Phase III sponsor. This shows that NOVA is striving to carry out research and development with the sole aim of bringing state of the art products into commercial market.

F. RELATIONSHIP WITH FUTURE R&D WORK

F. 1. Anticipated Results of Phase I and Phase II

The results of Phase I and Phase II work will be the development of a commercial smart tag system with remote controller and applicator. The tag will be manufactured on silicon and will be completely self contained not requiring any external antennas or batteries. It will have very small size and will be programmed and readout by a remote controller within a distance of ≥ 1 m. An applicator is proposed that will place the tag on the item inside a tiny non hardening glue ball which can be removed without affecting the surface of the item it is attached to.

F. 2. Significance of Phase I Work on Phase II Study

This project is proposed as an introduction to Phase II. During Phase I a small prototype will be designed, simulated, fabricated and tested. Therefore, the feasibility of the proposed smart tag system will be experimentally demonstrated. The results obtained from Phase I prototype will save valuable time during Phase II for developing the final commercial product. The applicator will be studied carefully and some experiments will be carried out. These results will be used to develop a commercial smart tag system during Phase II. During Phase III the completed tag system will be manufactured as a commercial product and supplied to government and commercial sectors. Phases II and III are estimated to take two years each to complete.

G. POTENTIAL POST APPLICATIONS

G. 1. Commercial Application

Potential commercial application of a smart versatile tag is self evident and extremely good. It can be applied to monitoring, tracking, searching, labeling, personalizing, selecting and finding

scattering and channeling in single crystals. He also performed research involving ultra-high vacuum technology using mechanical, turbal-molecular, ion, and titanium sublimation pumps. In addition he worked with low temperature technology using a cryo pump cryostat, and cold head. He has also developed the electronics for these projects. He will carry out most of the tasks listed in the work schedule.

Vice-president Dr. T.O. Tümer is the Co-Principal Investigator for this project. He will be responsible to NOVA for the successful conclusion of this project. He has 30 years experience in detector design, development and fabrication. Dr. Tümer has worked at NOVA since it was founded 12.5 years ago. He has over 75 publications in scientific journals and books, and many more reports, presentations and abstracts. He has supervised students and directed many research projects. He has extensive experience in fast electronics, ASIC chip development, gamma ray and particle detectors, Compton double scatter techniques and real-time data analysis. He has also extensive experience in silicon and CdZnTe strip, pad and pixel detectors and their applications. He is the PI of two Phase II contracts, one for DOD/BMDO for a space borne gamma-ray detector for gamma rays from 0.3 to 30 MeV and the other for DOD/Army on nondestructive inspection of munition items with x rays. He is also the PI of two new projects just been awarded on medical imaging; scintimammography and digital mammography. He will oversee the development and commercialization of the proposed smart tag system.

Engineer Dr. Scott Kravis, previous to employment at NOVA R&D, Inc., conducted research on highly-charged ion-atom collisions and photoionization of atoms and ions using synchrotron radiation. He has used and applied many radiation detectors and data acquisition systems. He build interface electronics for experimental control. He has also designed and built a high charge state low energy electron beam ion source (EBIS). He has developed all the electronics for these experiments. He has given oral presentations at international conferences and workshops on these topics. Since he came to NOVA, Dr. Kravis has been working on CdZnTe linear pad detector arrays and medical imaging systems. He is primarily working on image acquisition from these detectors through mixed signal ASIC chips and the testing and evaluation of the RENA chip. He will work on the smart tag chip design and optimization. He will also contribute to the design and development of the test and remote control electronics for the smart tag system.

Mr. Rene Brown founded Lasair Design and is the principal engineer and owner. Mr. Brown has 20 years of experience, 16 of which has been with Hughes Aircraft Company. He has designed circuits in silicon, germanium, and GaAs. He has designed 15 focal plane arrays for various applications. Mr. Brown has been involved in many high speed design projects at Hughes. Previous designs include high-speed ECL logic operating at 200 MHz, complementary JFET logic capable of 80 pico second propagation delays, low noise 3 GHz bandwidth low power amplifiers for CO_2 laser systems, a fiber optic receiver using a GaAs transimpedance amplifier and high speed CMOS logic (100 MHz) for infrared CCD imagers, HgCdTe and InSb detectors hybridized to CCD and CMOS readouts, germanium readouts using JFET circuits for amplifiers and logic, GaAs readout with a capacitive transimpedance amplifier using MESFET devices, and BICMOS readouts with differential or folded cascode preamplifiers. He has designed many digital logic circuits including designs in SOS, CMOS, ECL, and IIL logic. He has also investigated logic designed in Ferro electric, GaAs MESFETS, and germanium JFETS. He has designed analog integrated circuits for radiation hard requirements and has extensive test experience with circuits in cryogenic, gamma and x-ray environments. Mr. Brown has MS BS degrees in electrical engineering from the University of California at Davis. He has authored or co-authored seven papers on focal plane arrays and signal processing for focal plane arrays. Mr. Brown is a registered Professional Engineer in the State of California (E 11255). He will work on the silicon layout of the smart tag ASIC chip.

All members of the key personnel plan to take part in Phase II of this project, are totally committed and are determined to make the proposed project a great success.

ATTACHMENT 5

MATERIAL INSP[illegible]ION AND RECEIVING REPORT

Form Approved
OMB No. 0704-0248

PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES.
SEND THIS FORM IN ACCORDANCE WITH THE INSTRUCTIONS CONTAINED IN THE DFARS, APPENDIX F-401.

1. PROC. INSTRUMENT IDEN. (CONTRACT)	(ORDER) NO.	6. INVOICE NO./DATE	7. PAGE	OF	8. ACCEPTANCE POINT

2. SHIPMENT NO.	3. DATE SHIPPED	4. B/L TCN	5. DISCOUNT TERMS

9. PRIME CONTRACTOR CODE		10. ADMINISTERED BY CODE	
11. SHIPPED FROM (If other than 9) CODE	FOB:	12. PAYMENT WILL BE MADE BY CODE	
13. SHIPPED TO CODE		14. MARKED FOR CODE	

15. ITEM NO.	16. STOCK/PART NO. DESCRIPTION *(Indicate number of shipping containers - type of container - container number.)*	17. QUANTITY SHIP/REC'D*	18. UNIT	19. UNIT PRICE	20. AMOUNT

21. CONTRACT QUALITY ASSURANCE

A. ORIGIN

☐ COA ☐ ACCEPTANCE of listed items has been made by me or under my super- vision and they conform to contract, except as noted herein or on supporting documents.

DATE | SIGNATURE OF AUTH GOVT REP

TYPED NAME AND OFFICE

B. DESTINATION

☐ COA ☐ ACCEPTANCE of listed items has been made by me or under my supervision and they conform to contract, except as noted herein or on supporting documents.

DATE | SIGNATURE OF AUTH GOVT REP

TYPED NAME AND TITLE

22. RECEIVER'S USE

Quantities shown in column 17 were received in apparent good condition except as noted.

DATE RECEIVED | SIGNATURE OF AUTH GOVT REP

TYPED NAME AND OFFICE

** If quantity received by the Government is the same as quantity shipped, indicate by (✓) mark, if different, enter actual quantity received below quantity shipped and encircle.*

23. CONTRACTOR USE ONLY

DEPARTMENT OF THE ARMY
UNITED STATES ARMY TANK-AUTOMOTIVE AND ARMAMENTS COMMAND
ARMAMENT RESEARCH, DEVELOPMENT, AND ENGINEERING CENTER
PICATINNY ARSENAL, NJ 07806-5000

RECEIVED MAY 12 1997

REPLY TO
ATTENTION OF

AMSTA-AR-ASC/SBIR Program

SUBJECT: Invitation to Submit SBIR Phase II Proposal

06 MAY 1997

NOVA R&D, Inc.
1525 Third Street
Suite C
Riverside, CA 92507

Topic#: A96-009
Control #: A962-0417

Dear Sir/Madam:

Congratulations! Your company is invited to submit a Phase II Small Business Innovation Research (SBIR) proposal based on your Phase I project, "Low Cost Smart Tag & Applicator", Contract DAAE30-97-C-0012.

If you wish to continue in this process, please submit three copies of your Phase II proposal following the instructions found in Enclosure 1. Send your proposal to the following address:

Commander, US Army TACOM/ARDEC
ATTN: AMSTA-AR-ASC (Mr. John Saarmann)
SBIR Program
Building 1, Mailstop 3/4
Picatinny Arsenal, NJ 07806-5000

An additional copy of your proposal should be sent to the Army SBIR Program Office at the address listed in Section 2 of the proposal instructions. Copies of the forms for Appendix A and B (pages 1 and 2 of the proposal) are enclosed along with Appendix C (Cost Proposal) and Appendix E (Company Commercialization Report).

Phase II proposal submissions must be responsive to the instructions in Enclosure 1 and should be received no later than Friday, June 13, 1997, in order to be considered for SBIR funding.

Thank you for your continued participation in the Army SBIR program. If you have any questions, please feel free to contact me at (201) 724-7943 or by email at <saarmann@pica.army.mil>.

Sincerely,

John Saarmann

John Saarmann
ARDEC SBIR Administrator

Enclosures

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APPENDIX A

U.S. DEPARTMENT OF DEFENSE

SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM
PROPOSAL COVER SHEET

Failure to fill in all appropriate spaces may cause your proposal to be disqualified

TOPIC NUMBER: A96-009

PROPOSAL TITLE: Low Cost Practical MicroTAG™ and a Tag Applicator System

FIRM NAME: Nova R&D, Inc.

MAIL ADDRESS: Nova R&D, Inc.

1525 Third Street, Suite C

CITY: Riverside STATE: CA ZIP: 92507

PROPOSED COST: $749,730 PHASE I OR II: II PROPOSAL PROPOSED DURATION: 24 IN MONTHS

BUSINESS CERTIFICATION:

	YES	NO
► Are you a small business as described in paragraph 2.2?	☒	☐
► Are you a socially and economically disadvantaged business as defined in paragraph 2.3? (Collected for statistical purposes only)	☐	☒
► Are you a woman-owned small business as described in paragraph 2.4? (Collected for statistical purposes only)	☐	☒
► Have you submitted proposals or received awards containing a significant amount of essentially equivalent work under other DoD or federal program solicitations? If yes, list the name(s) of the agency or DoD component, submission date, and Topic Number in the spaces below.	☐	☒

► Number of employees including all affiliates (average for preceding 12 months): 11

PROJECT MANAGER/PRINCIPAL INVESTIGATOR	CORPORATE OFFICIAL (BUSINESS)
NAME: Dr. Jianping Peng	NAME: Dr. Tümay O. Tümer
TITLE: Research Physicist	TITLE: Vice President
TELEPHONE: (909) 781-7332	TELEPHONE: (909) 781-7332

For any purpose other than to evaluate the proposal, this data except Appendix A and B shall not be disclosed outside the Government and shall not be duplicated, used or disclosed in whole or in part, provided that if a contract is awarded to this proposer as a result of or in connection with the submission of this data, the Government shall have the right to duplicate, use or disclose the data to the extent provided in the funding agreement. This restriction does not limit the Government's right to use information contained in the data if it is obtained from another source without restriction. The data subject to this restriction is contained on the pages of the proposal listed on the line below.

PROPRIETARY INFORMATION: Pages 3 to 49

SIGNATURE OF PRINCIPAL INVESTIGATOR	DATE	SIGNATURE OF CORPORATE BUSINESS OFFICIAL	DATE
	8/6/97		8/6/97

U.S. DEPARTMENT OF DEFENSE

SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM
PROJECT SUMMARY

Failure to fill in all appropriate spaces may cause your proposal to be disqualified

TOPIC NUMBER: A96-009

PROPOSAL TITLE: Low Cost Practical MicroTAG™ and a Tag Applicator System

FIRM NAME: NOVA R&D, Inc.

PHASE I or II PROPOSAL: Phase II

Technical Abstract (Limit your abstract to 200 words with no classified or proprietary information/data.)

A Phase I feasibility study on a low cost practical smart tag chip (MicroTAG™) and a MicroTAG applicator has been completed. The first prototype version of the proposed MicroTAG chip was designed and fabricated. The preliminary tests carried out on the MicroTAG chip were successful, but not all functions have been tested yet due to the Phase I funding limitations. The prototype MicroTAG chip will be fully tested during Phase II, and a second (if necessary a third) version will be designed and fabricated. A remote programmer/reader (interrogator) will also be developed. The resultant MicroTAG chip and the interrogator are expected to be ready for fabrication at the end of Phase II.

A novel applicator for the MicroTAG chip is also developed. The first version was designed and fabricated as proposed. The prototype, which is a manual applicator, is designed to apply MicroTAG onto any type of package, bag, box, luggage, and crate of various thickness and stiffness while they are transported on a conveyor. The MicroTAG chip will be applied to the item as it is moving with arbitrary order, shape, size, orientation and position. The conveyor can reach maximum speed of two hundred feet per minute. The material covering the item can be cloth, metal, plastic, paper, or wood. The results obtained demonstrate the feasibility of the MicroTAG applicator. The applicator will be modified, improved, and optimized during Phase II. An automatic version will be designed and fabricated. The MicroTAG chip applicator is expected to be ready for manufacturing at the end of Phase II. In Phase III, MicroTAG, remote programmer/reader system, and the MicroTAG applicator will be commercialized.

Anticipated Benefits/Potential Commercial Applications of the Research or Development.

The result of the Phase II program will be a practical low cost smart tag, a remote programmer/reader system and a versatile applicator. The MicroTAG can be used in many different applications. The applicator can be used to tag any type of conveyor-transported item. They can also be used separately or together in many other applications where manual/automatic tagging is needed.

List a maximum of 8 Key Words or short (2-3 word) phrases that describe the Project.

Tags	Smart Tags
Remotely programmable tags	Tag applicator

Table of Contents

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A IDENTIFICATION AND SIGNIFICANCE OF THE PROBLEM

A. 1 Problem

Smart tags are presently used for a number of applications in both the civilian and military sectors. These applications include item identification, toll passes, and barrier tagging. These tags are relatively expensive, costing several dollars, and are limited in the amount of information they can store. These tags cannot be used in large quantities, because of the cost involved, especially in circumstances where they can not be recovered for reapplication.

Both military and civilian sectors require low cost tags costing few cents each for many different applications especially for use in large quantities where tag recovery is impractical. Some applications for Government use include tagging individual weapons, munitions or pieces of equipment, crates, and other inventory. Some civilian applications include tagging baggage in airports, parcels, packages, crates, individual items, files, folders, and dockets, inventory, shop merchandise, and for employee and vehicle identification.

Tagging baggage at airports is an important application. It will be beneficial to have a smart baggage tagging system which can store detailed information. This will allow to track the history of baggage: point of origin, travel route, and a profile of the owner. Such information will require significant amount of non-volatile memory.

The size of the tag is also important so that it can be placed onto baggage and cargo inconspicuously. Therefore, the size of the tag should be smaller than about $5 \times 5 \times 0.3$ mm^3.

The tag should not require any external power or antenna. Even a tiny battery or a small antenna will increase the size and complexity due to the connection of the battery and/or the antenna to the chip; at the same time tag's cost increases dramatically. A battery has a finite lifetime and the probability of failure during application is greater. A tag with the required power generated on board by the remote programmer/reader would be a better solution for accommodating power needs.

Development of such a smart tag requires a suitable applicator. The applicator must be simple in design and cost-effective. The applicator must be able to apply the smart tag onto any type of package, bag, box, luggage, and crate of various thickness and stiffness while they are transported on a conveyor. The applicator must apply the tag onto the baggage item as it is moving with arbitrary order, shape, size, orientation, and position. It must work fast, as the conveyor can reach a maximum speed of one meter per second with about one meter spacing between each item. The tag must adhere easily to different kinds of luggage material such as, cloth, metal, plastic, paper, leather or wood.

A Phase I program is completed and the feasibility of a practical low cost smart tag and a novel applicator has been studied and demonstrated.

A. 2 Present State of the Art Regarding Smart Tag Chips

Figure 1 shows the reproduction of an article in EDN magazine (June 19, 1997) that presents recent progress in the area of radio-frequency identification (RFID) tag chips. The size of the tags shown is $61 \times 10 \times 0.1$ mm^3 (610 mm^2 area), which obviously makes them unsuitable for the kind of automatic application planned for this proposal. In the case of SCS Corp.'s tag chip shown in Figure 1, the size of the RF antenna needed for the communication between tag chip and remote programmer/reader places a limit on the reduction in size that can be achieved. By using higher frequencies and carefully investigating the antenna design, we hope to overcome this limitation. The size of the present prototype MicroTAG chip is 16 mm^2 (future versions expected to be ≤ 9 mm^2) which is nearly 40 times (or ≥ 68 times) smaller than the SCS Corp. tag chip. The SCS chip also requires mounting the antenna onto the chip where *NOVA*'s MicroTAG chip will have both the transmission and receiving antennas on chip and will not require any mounting. Another aspect that we plan to improve on is the price of the SCS Corp. chip, which is quoted to be $0.95 each.

RFID tags shrink and gain flexibility

Radio-frequency identification (RFID) takes a new form in the Interactive Identification (I^2) technology from SCS Corp. Except for the tiny bulge of an embedded IC, an I^2 RFID tag looks and feels like a short strip of flexible plastic tape. Each 2.4×0.4×0.004-in. tag receives and transmits data at 2.4 GHz without a battery, using on-chip circuitry to convert and store energy from received signals' carrier waves. Read and write distances are nominally a foot or so, but they can be considerably greater, depending on the power transmitted by the scanner unit that reads and writes to the tags.

The I^2 tags owe their size to their 2.4-GHz operating frequency, which allows printing an antenna on each flexible tag. In contrast, RFID tags that operate at lower frequencies require embedded coil antennas. For reliable operation, the I^2 technology uses frequency-hopping spread-spectrum techniques similar to those of wireless LANs. You need an FCC license to use some ac-operated scanners, but you can use low-power, handheld scanners without a license.

These flexible, plastic I^2 RFID tags from SCS operate without a battery and can send and receive data over distances of a foot or more.

Both types of scanners are available from SCS. SCS envisions that the tags will find use in baggage-handling, parcel-tracking, and uniform-rental applications. (The tags can be sewn into the seam of a garment and can withstand commercial laundering.)

Each tag's 1 kbit of antifuse memory allows storing and updating information that could include ownership, itinerary, a record of operations, control codes, and so forth. SCS says the CMOS technology it developed for the tags allows programming with only 4V and microamps instead of a typical 8V and milliamps for conventional programmable logic. In addition, read and write times are nominally 4 and 9 msec, respectively, for a 16-bit word—short enough to allow nearly simultaneous processing of multiple tags. An I^2 tag costs $0.95 (100,000). A development kit, including a scanner, software, and 1000 tags, costs $4500.—by Gary Legg

SCS Corp, San Diego, CA. 1-619-485-9196, fax 1-619-485-0561.

Circle No. 499

Figure 1: Reproduction of a short article showing the present state of the art in RFID (tag) chips (from EDN magazine, June 19, 1997)

B RESULTS OF PHASE I WORK

B. 1 Introduction

During Phase I an ambitious attempt was made to design and fabricate a prototype limited function tag chip, since a simulation study is normally not sufficient to demonstrate feasibility of a complicated chip such as *NOVA*'s MicroTAG chip. The MicroTAG chip was successfully simulated and designed during Phase I and fabricated. The simulation study and silicon layout took longer than we have anticipated and we had to request a three month no-cost extension on our Phase I work. However, fabrication of a prototype tag chip during Phase I will help the development of a commercial version during Phase II significantly. We expect that it will also save about 6 to 9 months of time during Phase II and enhance its prospects for a successful conclusion. The fabrication of a successful MicroTAG chip will also complement *NOVA*'s Automatic Baggage Inspection System (ABIS) development work.

NOVA has also studied, designed, and developed a low cost tag applicator system during Phase I. This system is required for mounting tags onto baggage scanned by a scanner system. A novel glue based system is used where the tag chip is embedded inside a drop of molten glue and propelled onto the baggage using air pressure. The glue used is a new type that has good adhesion but stays reasonably soft and does not affect the surface it is applied to. The resulting glue-chip pellets are small, transparent, and inconspicuous.

NOVA expects that, if successful, the tag chip and tag applicator will be deployed with the ABIS system. *NOVA*'s tag chip and the tag applicator can be used for numerous other applications. Especially the tag chip is designed to be versatile and the commercial application possibilities are endless.

B. 2 The Prototype MicroTAG™ Chip

B. 2. 1 Design of the MicroTAG chip

A practical smart tag (MicroTAG) chip built on a tiny silicon die as proposed in the Phase I proposal has been designed, simulated, and fabricated. The size of the MicroTAG chip developed is 4 x 4 x 0.3 mm^3. The MicroTAG chip is designed to be completely self-contained. The prototype chip designed and fabricated during this project contains connection pads for testing. The final chip ready for manufacture at the end of Phase II will not contain any connections pads and its size will be significantly reduced to ≤ 9 mm^2. It contains two antennas placed on opposite sides of the chip (Figures 9 to 11). One of them receives the microwave signal from the interrogator which is used both to power the chip by storing charge onto a large on-chip capacitance bank and to transmit data to the chip. The second antenna is used to transmit the chip's response to any data requests from the interrogator. Rather than using an active transmitter (which would require a large amount of power) for this purpose, this antenna is set up in the Phase I design to reflect a continuous wave from the interrogator with varying efficiency; the data from the chip is encoded in the pattern of the efficiency variation. For details of this "modulated backscatter" design see the discussion given below. For the Phase II design we plan to use the same principle, although we will likely have to add spread-spectrum techniques in the final design to increase the noise immunity of the system.

A computer aided design (CAD) program developed for modeling and simulating electromagnetic devices has been used during Phase I. Same program is expected to be used during Phase II. This program is especially useful to design and simulate the receiving and transmission antennas. In this work the spacing and thickness of the antenna metal will be optimized for application to the proposed MicroTAG chip. For example, the present prototype has been designed for 10 GHz where the microwave skin depth is about 0.8 micrometers to achieve low resistivity. The skin depth is the distance the microwave currents penetrate into the surface of the metal layer. It is within this characteristic depth that the electromagnetic field propagates. This skin depth varies with the frequency and dielectric constant of the surrounding media. The test results from the first version will be used during Phase II to fully optimize the MicroTAG chip design.

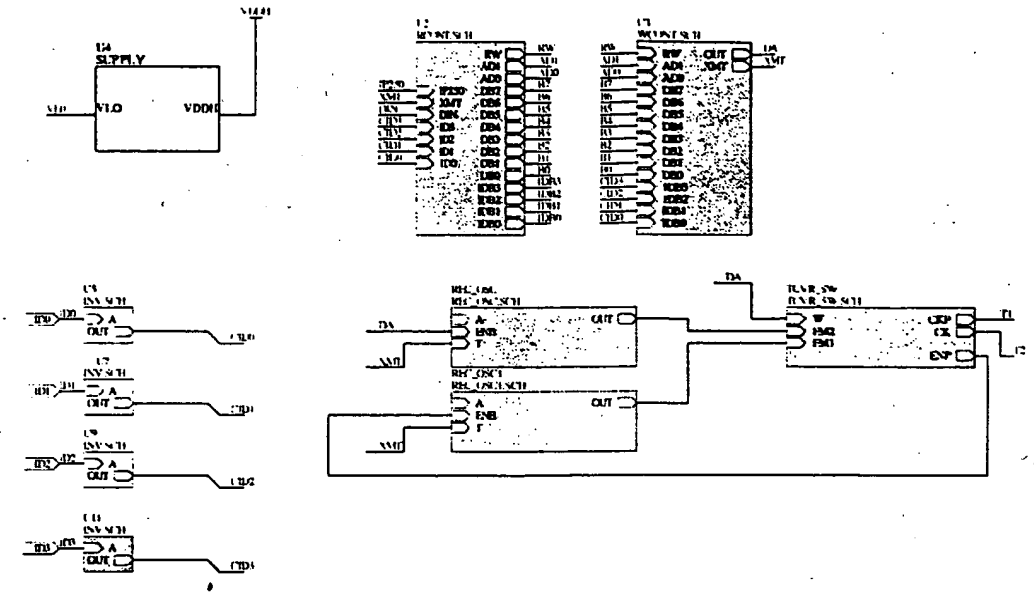

Figure 2: Top level schematic layout of *NOVA*'s MicroTAG chip.

The top level schematic diagram of the MicroTAG chip developed during Phase I is shown in Figure 2. For this version, it consists of four sections: The left block is the power supply (SUPPLY), the middle block is the read-in and memory section (RCONT), and the right block is the transmit section (WCONT). The lower right blocks are the oscillators that modulate the backscatter transmitter.

The chip is powered by charging a capacitor array, either via microwaves sent from the stationary transceiver that will be part of the MicroTAG system, or for this test version through a pad on the chip. For diagnostic purposes, the pad can be activated and deactivated by a gate that is controlled via a second pad. The charge state of the capacitor array is output through a source follower, again for test purposes. Of course, this source follower is powered separately from the main chip circuits, as are all other diagnostic circuits, to avoid any interference with the chip tests.

The four chip ID inputs are shown in the lower left. Eventually, the ID codes will be fixed in metal or programmed onto suitable ROM circuitry for various versions of the die. For the first test version, an external, programmable capability was thought to aid diagnostics. These four ID bits are programmed by the off chip control to be any value we choose. 16 codes are possible for this version. A default code is generated by pull-up and pull-down resistors on the ID inputs. Other pads on the chip allow us to access information from various stages of the data processing on the chip. For example, when transmitting data to the chip, we can bypass the antenna and directly send the data to a serial input pad instead, freeing us from the need to worry about the actual microwave transmission at this stage. Also, we can examine whether the information written to the latch registers (cf. the discussion below) and the memory agrees with the data transmitted through the serial input. The relevant pads are set up as bidirectional pads to allow both read and write access. This enables us to test parts of the circuit even if other parts that come earlier in the data processing sequence turn out not to work as intended.

The read control section is shown in Figure 3. The data is serially transmitted to the chip by frequency-modulating the carrier wave (typically 10 GHz) with a frequency of 1 MHz for low signals (logic 0) and with 10 MHz for high signals (logic 1). On the chip, the incoming signal is demodulated and then sent through a high-pass filter. The output from this processing stage (not shown in Figure 3) is applied to the DIN input. That signal is modulated to be either at a 25% or

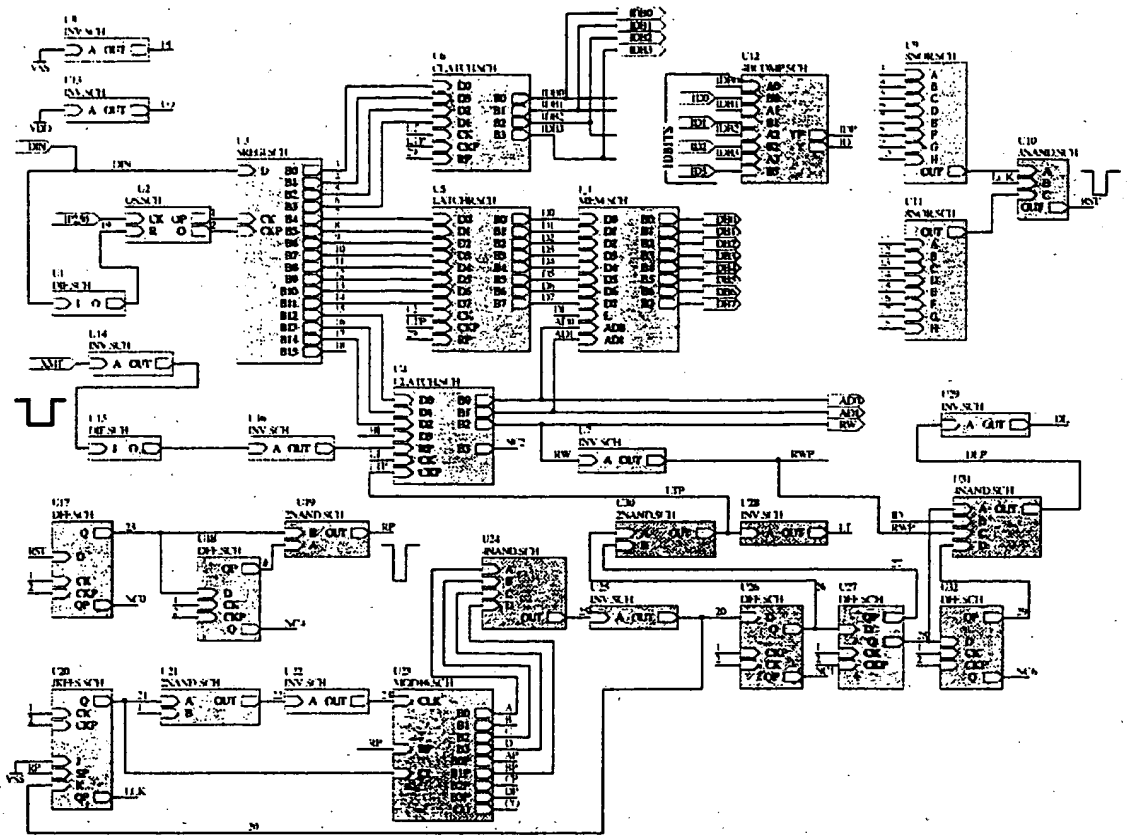

Figure 3: Read control section.

75% duty cycle. The first 25% of the waveform is always high and the last 25% is always low. The input data determines if the 50% point on the waveform is a logic 0 or a logic 1 (if the signal is 25% duty cycle or 75%). The clock is recovered by determining the rising edge of the input signal with a digital differentiator (U1) and triggering a one-shot (U2) to the 50% time point. The signal level that is present at the input of the shift register U3 when the one-shot resets is loaded into the register. The output from one-shot U2 also provides the master clock for the flip flops and counters in the read control section. Its width is determined by an on-chip current source formed by the leakage current through a series of MOSFETs. Since this width is only used to distinguish between a 25% and a 75% duty cycle, the control current is not a critical parameter.

The SREGI block (U3) is the input shift register. It is a simple D type register with 16 cells. U4, U5, and U6 are simple D latches. They latch the data for the time required to see if a transmit command is being asked for or if the ID bits transmitted in the data stream agree with the chip ID, allowing the data to be written to memory. The latches are clocked 16 counts after a "1" is sensed in the data. In order to have a well-defined start of the data sequence, any data transmission to the chip must be preceded by an all "0s" state (16 bits). The first data bit then has to be a logic 1. This triggers the "OR" gate U9, 10, 11 and generates the RST command which starts a digital one-shot. Once the one-shot is fired, the LCK command prevents the RST command from operating again until the cycle has timed out. The 16-bit counter MOD16 (U23) controls the state of the read control section after a valid initiation pulse sequence is detected.

The RST command is normally low and therefore a logic 0 is normally clocked into D Flip Flop U17. This ripples into U18 and set RP normally high. When RST first goes high indicating the first

presence of a logic 1 in the data, a logic 1 is clocked in U17. Then for one count, RP goes low, then goes back high. (RP only occurs on a low to high transition of the RST signal again explaining the requirement for an all "0's" condition to precede a real data set.) RP synchronously resets the MOD16 counter and triggers the JKFF that controls the digital one-shot.

The digital one-shot consists of U20, 21, 22, 23, 24, and 25. It is triggered by the RP command. It could be retriggered in the middle of a count due to the RP reset of the counter, but the lockout on the RST command keeps this from happening. Once triggered, node 21 goes high allowing the AND gate U21, 22 to send clocks to the counter. An additional (redundant) lockout is provided by node 21's control of the count input of the counter. A 4 input NAND gate is used to decode the count on which the one-shot times out. This is needed since the U17, 18 RP generator takes a few clock cycles to generate RP; those cycles must be subtracted from the 16 total counts required. D flip flop U26 (clocked on the falling edge of the master clock) is used to deglitch the output of the AND gate U24, 25 and to provide a clean input into the control signal generators U27 and U32. LT and DL are generated from the terminal count of the digital one-shot in the same way that the RP signal was generated from RST.

Write Cycle

When the LT command latches the digital word into the latches, the digital comparator U12 is used to compare the chip ID sent with the data stream to the hardwired chip ID bits on the die. If they match, the ID signal goes high enabling the DL signal. The Read/Write signal (RW) has to be low for the DL signal to go high. This requirement ensures that the memory is not overwritten by a transmit request (RW=1), only when sending data to the chip (RW=0). With all these conditions satisfied, data can be entered into the memory using the latched data and address applied to the memory block.

Note that the U5, 6 latches are reset by node 29. This keeps unwanted data from being inadvertently loaded into memory. Once the data is tested and conditionally used, it is erased.

Transmit Cycle

If RW is a logic 1, DL will not occur and no data will be latched into the memory. The address bits are, however, applied to the memory block, so whatever is in the selected memory controls the memory output bus. This provides the stimulus and data needed to start the transmitter sequence.

The XMT command is high during the transmit cycle. This signal is brought into the read control block to reset the address and latched RW signal on its falling edge, i.e., after the transmit cycle ends. This keeps the cycle from retriggering itself and hogging the RF I/O until the energy stored in the supply is gone.

The write control section is shown in Figure 4. Once enabled by appropriate commands, this section grabs data from the memory data bus, pulse-width modulates it in the same manner as the input signals were, and sends it out serially on the OUT line. As is the case with the data transmitted to the chip, an "all 0's" condition must precede the actual data, followed by a bit 1 to indicate the start of the data word. Therefore, MUX U1 first outputs zeros for the first 16 counts and then outputs data for the last 16 counts.

Another RP generator U20, 21 is part of this section. It is triggered by the rising edge of the RW command. The rising edge is determined by the digital differentiator U23, 24.

Since the pulse-width modulator divides the data output into four time periods, and 32 data bits are output during the transmit cycle, at least 128 counts are needed in the digital one-shot. Since there are various delay sources in the write control block, a 256-bit counter (MOD256) was used to

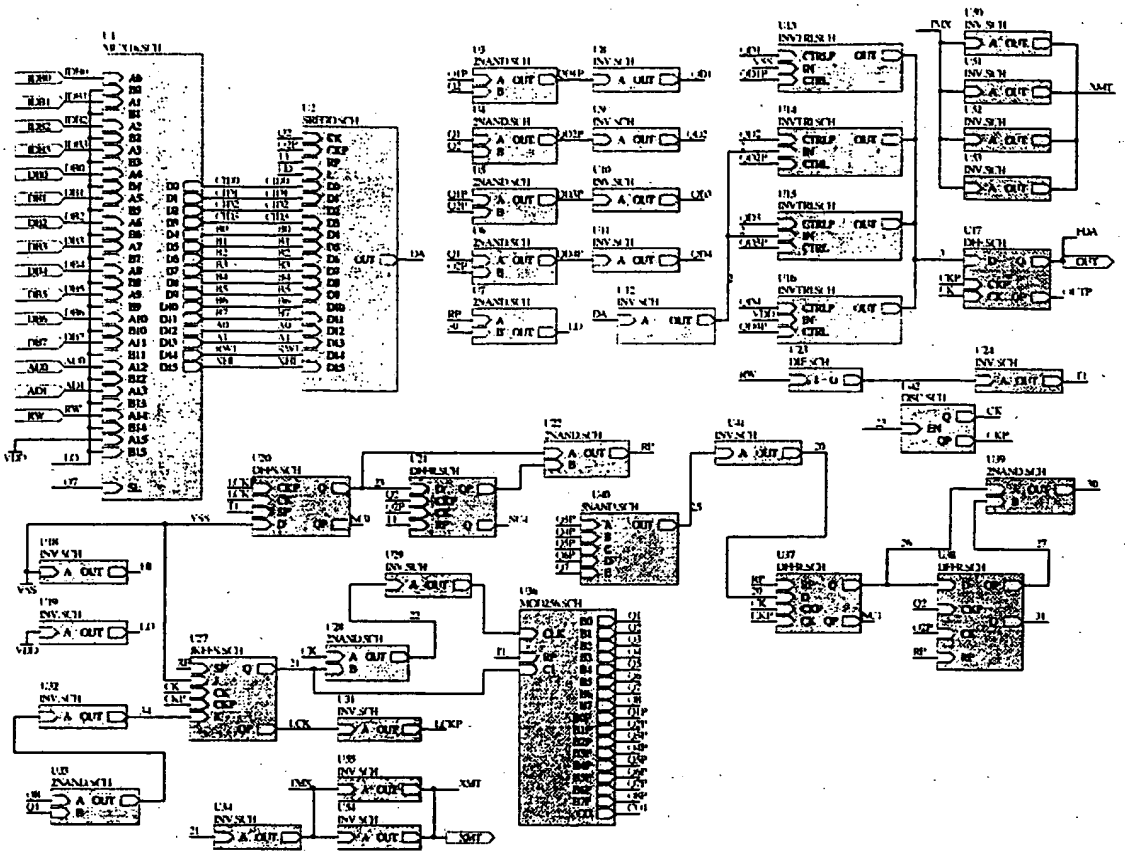

Figure 4: Write control section of the MicroTAG chip.

align the timing. While some logic optimizations may be possible in this implementation, we consider the design to be both solid and functional.

Oscillator block U25 generates the on-chip clock. It is implemented as a simple gated ring oscillator. This was done (as opposed to charging and discharging a capacitor with a current source) to reduce power dissipation on the die.

At the appropriate time the AND gate U40, 41 sends a command pulse down the U37, 38 flip flops, generating the node 30 signal. Both this and the local RP command are normally high. When either of them goes low for one clock cycle, the NAND gate U7 sets LD high for that time, loading data from the multiplexer into the parallel-in serial-out shift register U2. RP loads the initial load of 16 zeros from the B inputs of the MUX into the SR, and the LD command caused by node 30 going low loads the data.

The data appears at the DA output of the shift register and is sent to the pulse-width modulator U12–U16. A set of AND decoders provides successive time periods QD1, 2, 3, 4. The QD1 signal outputs a logic 1, the data appears at times QD2 and QD3, and a low is applied during time QD4. This again results in a 25% duty cycle for logic 0 and 75% for logic 1, while providing a rising edge for each bit, to facilitate the synchronization between transmitter and receiver.

Depending on the signal level at the DA output, one of the two receive oscillators shown in Figure 2 is then enabled and selected. These oscillators are tuned to frequencies of 1 and 10 MHz respectively. At that frequency, they will drive a dipole antenna between a half-wave and quarter-wave reflector. The frequency will be picked up by the stationary receiver as an intensity modulation of the backscatter by the antenna. This eliminates the need for a power-consuming active transmitter on the chip.

Miscellaneous Functions

In this section, we describe some of the more relevant individual circuits on the MicroTAG chip. Some of these circuits were deemed important enough to include stand-alone test versions on the edge of the die.

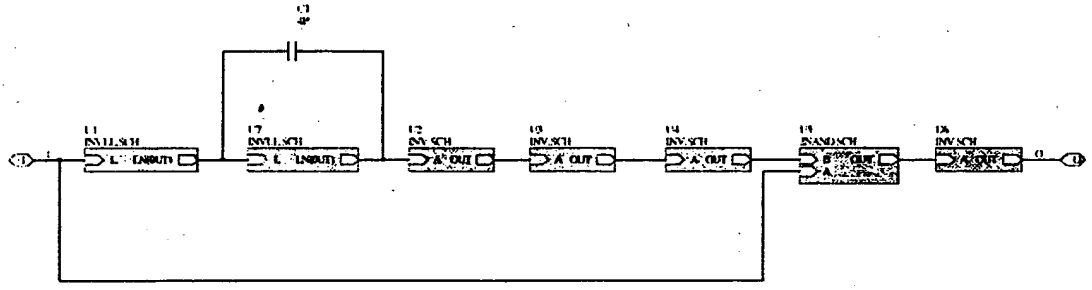

Figure 5: Digital differentiator circuit.

Figure 5 shows a simple digital differentiator. Its purpose is to provide a short output pulse when it detects the rising edge of an input clock. The output pulse width is determined by the delay difference between the two signal paths to the two-input NAND gate. The "L" style inverters have been made with a longer (10 μm) gate length. When this higher resistivity inverter drives the bridging capacitance, the delay path is deliberately lengthened. The present design outputs about a 100 ns pulse when triggered. In addition to being part of both the read and write control units of the MicroTAG ASIC, a separate test version of the differentiator was placed on the chip.

The retriggerable one-shot is shown in Figure 6. This circuit uses an input set current to program the one-shot's output pulse width. A logic high on the R input triggers the one-shot by turning M3 on, thus connecting the integration capacitor C1 to ground (V_{SS}) and setting node 2 high via the inverter M4, M5. As soon as R goes back to a logic low, the set current starts charging C1. As the voltage on the capacitor reaches the threshold of the inverter, the output pulse is stopped. The pulse width is set to about 50% of the incoming signal's period, so the one-shot, in conjunction with the differentiator, provides the required distinction between logic 1 and logic 0 in the input data, as discussed above. The corresponding set current is about 250 nA. Again, a separate test copy of the one-shot is implemented on the chip. For this circuit, the set current is supplied externally by connecting the appropriate pad (labelled IP250N in Figure 6) to ground through a suitable resistor. Since the input point is held 1 V below V_{DD} by the transistor M1, the ratio of that voltage to the resistance determines the current.

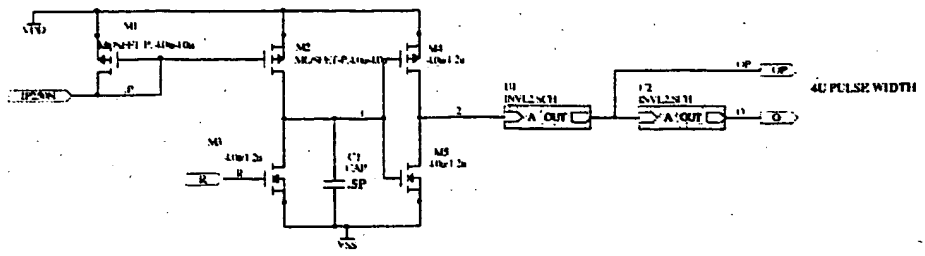

Figure 6: One-shot (monostable multvibrator) circuit.

The oscillator that provides the clock during data transmission from the chip is shown in Figure 7 It is a gated ring oscillator whose period is extended beyond the propagation delay of its three gates by bridging the two-input NAND gate with a 3 pF capacitor. The resulting frequency is still more than twice as high as the 100 kHz of the input signal. This means that the transmission can be completed before the read control circuit is reset by the next sequence of 16 zeros. Consequently, the timing of the data transmission to the chip can be simplified by not having to wait for the transmission from the chip to complete. (This, of course, requires that the stationary transceiver is set up in such a way that any possibility of interference between the two signals is eliminated.) There is a separate test version of this circuit too.

For the final version of the MicroTAG chip it is planned to use ROM circuits to store the relevant data permanently, independent of a continuous power supply. To program these ROMs, a higher voltage than the one supplied to the rest of the chip will be needed. To generate this higher voltage, we plan to use a charge pump similar to the one shown in Figure 8. Though the present version of the chip does not contain any ROM circuitry, we placed a test version of this charge pump on the chip in order to investigate the concept.

Two photographs of one of the finished chips and the chip layout are shown in Figure 9 to Figure 11 respectively, on the following pages. The layout shows the various individual test circuits (1), the read (2) and write control sections (3), the shift registers and memory (4), the backscatter antenna (5), the capacitor array for power storage (6), and the receiving antenna (7).

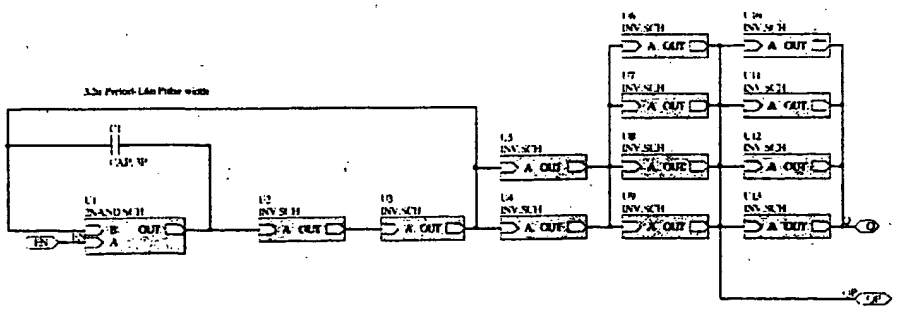

Figure 7: Oscillator circuit.

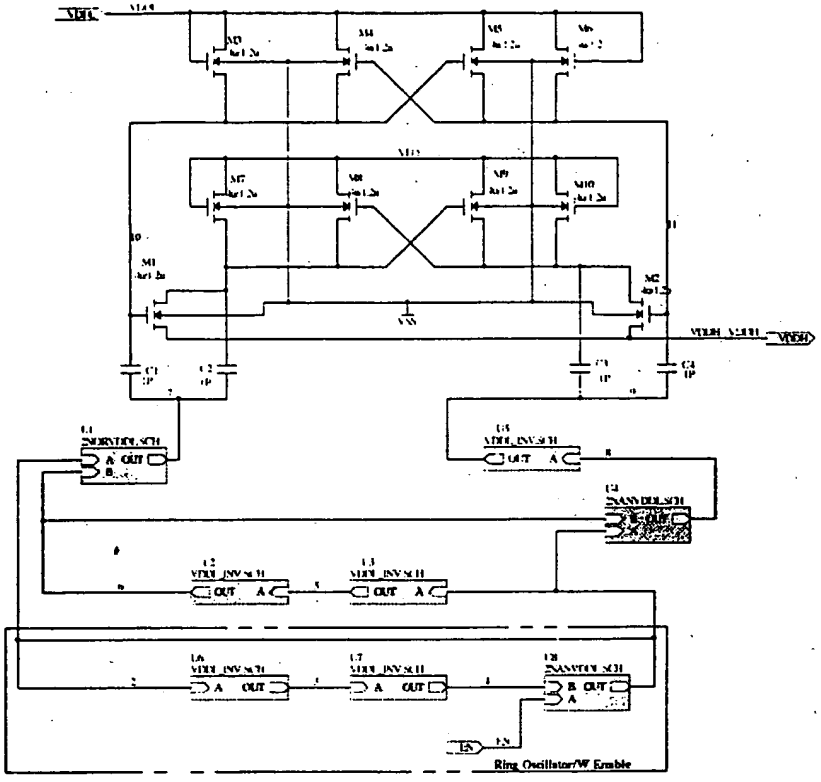

Figure 8: Charge pump circuit.

Figure 9: Photograph of the MicroTAG chip, showing its size in comparison to a dime.

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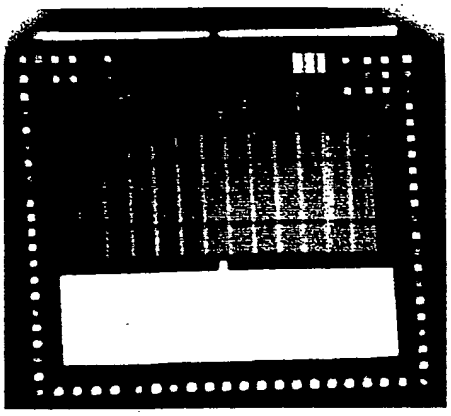

Figure 10: Photograph of the tag chip, taken under a microscope. In the picture, the chip appears at about 12.5 times its original size.

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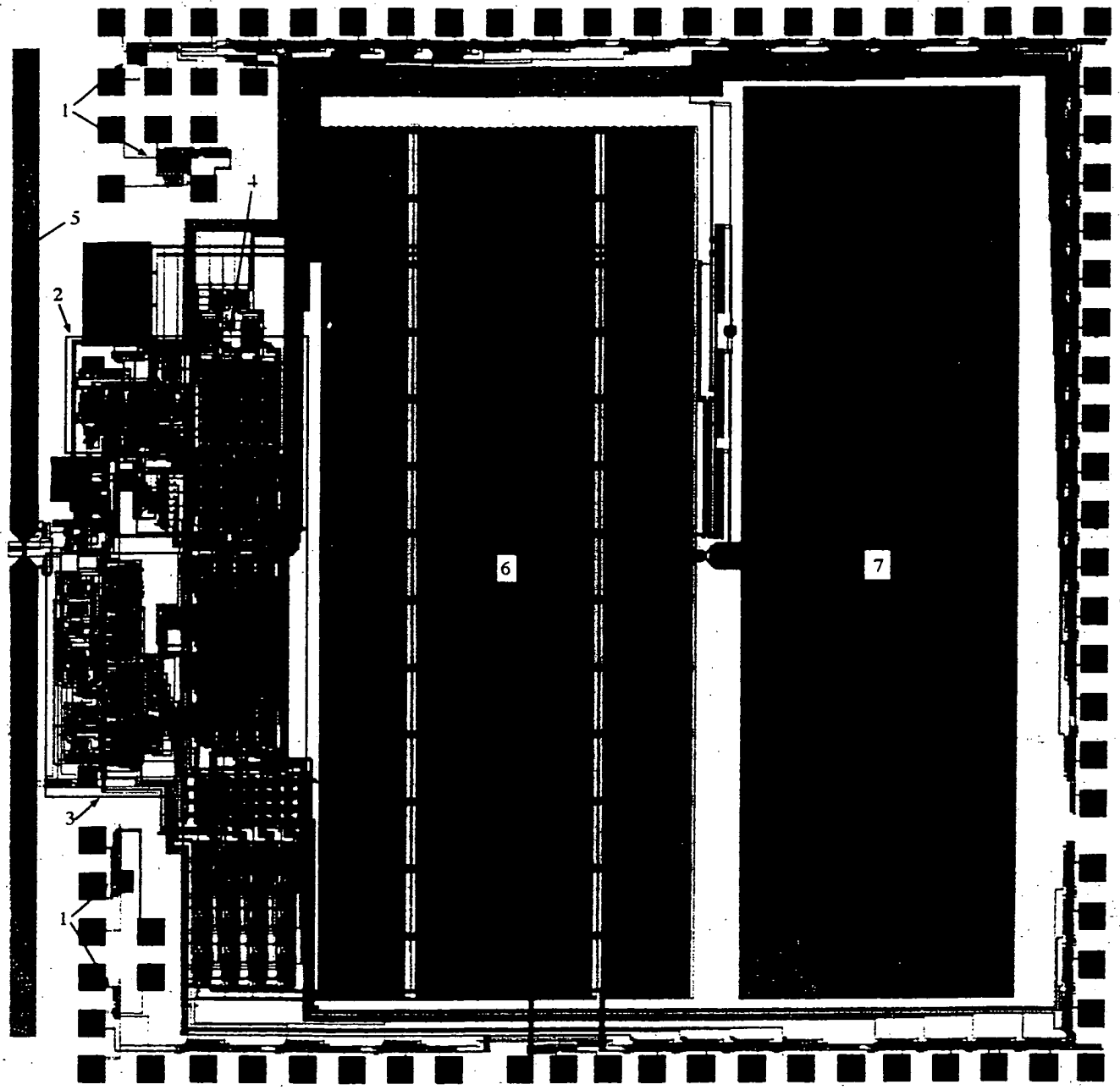

Figure 11: Layout of the tag chip. The numbers indicate the main parts of the tag circuit. 1: the various individual test circuits; 2: the read and 3: write control sections; 4: the shift registers and memory; 5: the backscatter antenna; 6: the capacitor array for power storage; 7: the receiving antenna.

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B. 2. 2 Performance of the MicroTAG chip

About two weeks after submitting the chip layout to the foundry for the prototype production, the chip layout engineer noticed that in the final editing a pad had inadvertently been left in a place where it would short one of the power supplies to ground. His attempts to correct this oversight before it would affect the production were unsuccessful. Fortunately, the short circuit could be eliminated by cutting the pad and one of the traces affected with a laser beam. The circuits that were supposed to receive their power through that trace had another, redundant connection to the power supply. The laser cutting, however, delayed the delivery of the chip by one week, correspondingly reducing the time available for testing. Moreover, the cutting process was unsuccessful for the first six chips that were cut. Of the remaining six chips, five were cut, while one was left unmodified as a backup. Another consequence of this layout error was that the differentiator test circuit was not connected to its output pad, so it could not be tested.

Another problem in the tests was the connection of the chips to our test circuit board. The chips were packaged in a pin grid array with a footprint for which we could not obtain a suitable socket in the time available. As a provisional solution, we used pin strips in the right arrangement to socket the chips. This, however, had the drawback that the contacts were not reliable. For example, most of the time the pad that gates the chip power supply did not contact well to the corresponding switch on the test board; fortunately, that meant that the gate was permanently open.

As a consequence of these restrictions, the following results should be regarded as preliminary.

The one-shot circuit (Figure 6) was tested by sending short pulses from a pulse generator to its input. These pulses were about 200 ns wide, with a repetition rate of about 150 kHz and an amplitude of 5 V. They are shown in trace 1 of the oscilloscope screen dump displayed in Figure 12. The circuit's response to these trigger signals is shown in trace 2 of the same figure. Four of the five chips tested showed a similar response, both in pulse width ($\approx$ 1.7 µs beyond the end of the trigger pulse) and amplitude (between 4.5 and 5 V). The fifth chip just output a 5 V DC level, possibly indicating that the charging of the capacitor did not work in this case. In order to compare the observed pulse width to the design value of 4 µs, the measured value has to be scaled by the ratio of the current used to charge the capacitor (about 400 nA) to the design current of 250 nA. Taking this into consideration, the measured pulse width corresponds to about 70% of the design value.

The oscillator test circuit was tested by connecting its power supplies to 5 V and ground respectively and setting its enable input (EN in Figure 7) alternatively low or high. With EN low, three of the chips performed as expected, giving a low signal level (logic 0) at the Q output and a high level (logic 1) at QP. The other two circuits gave the same level at both outputs, 5 V in one case and 0 V in the other. Unfortunately, none of these results changed when the enable input was high. Using a microprobe, we verified that the enable voltage did get through to the correct pin on the chip carrier, so the connection problems caused by our provisional socket could be excluded as an explanation for our failure to observe an oscillation. This leaves the connection from the pin to the actual input of the NAND gate, or problems with the capacitor. A third possibility, a malfunction of the NAND gate itself, seems less likely, as the results with EN low indicate that at least in principle the gates work. The chip that gave a low signal at both outputs was later investigated under a high-power (1000x) microscope. We found that the trace supplying the V_{DD} (5 V) power to the circuits had fused off the substrate at one point. The reason for this is under investigation. Since the control switches for the bidirectional pads for about half the chip use the same power, those are affected by this defect too.

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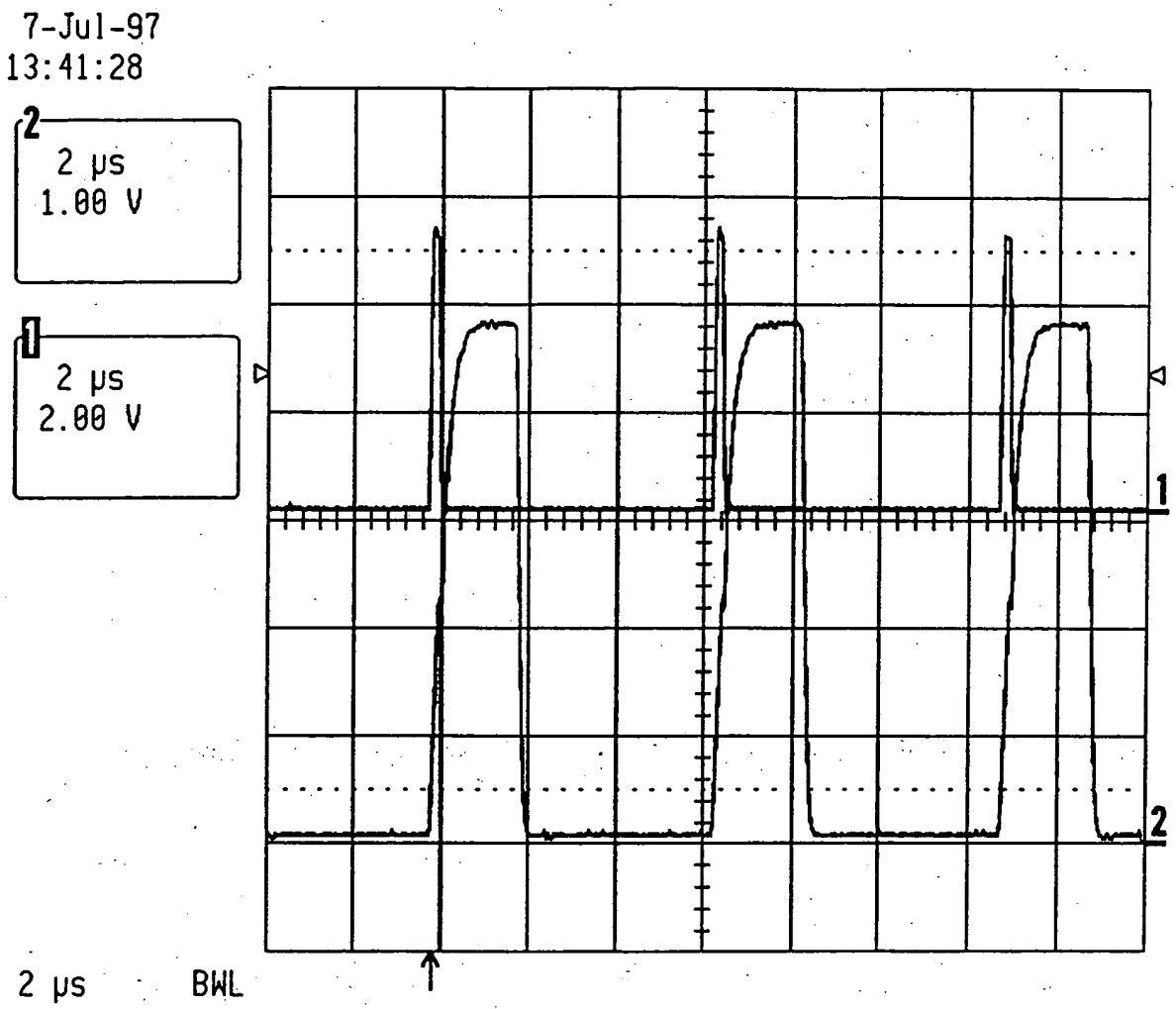

Figure 12: Test results for the one-shot. The input signal is shown in trace 1, the circuit's response in trace 2.

Next, we connected the power supply for the main MicroTAG circuit. As discussed above, a bad connection prevented us from supplying the voltage needed to control the gate for this supply directly through our test circuit. We were, however, able to supply this voltage directly to the chip carrier, again using a microprobe. When we did this, we could actually see the voltage on the capacitor array go down, as expected, in two cases. The other three chips were not affected by the control voltage.

At this point in the test sequence, one chip was taken for closer, microscopic inspection, as discussed above. We then supplied 2 µs wide pulses (50 kHz repetition rate) to the serial data input of the chip (DIN in Figure 3) and tried to observe the recovered clock signal from the differentiator/one-shot combination U1, U2 by probing nodes 1 and 2 of the read control circuit (cf. Figure 3). Two of the chips showed no "reaction" to the data, i.e., the level at node 1 was constantly low, while the

level at node 2 was high. In the third case, node 1 was constantly low too, but node 2 was an exact copy of the data input. Even when we varied the width of the input pulses, the width of the output varied correspondingly. This indicates that rather than the output from the one-shot, we were observing a short circuit between DIN and node 2. Finally, the fourth chip gave us a signal on node 1 that was normally at 2 V and went down to 0 for 1 μs in response to an input signal on DIN. The signal on node 0, on the other hand, was normally at 0 and went up to 3.5 V for 1 μs in response to an input. While the pulse duration was shorter than expected, indicating that the on-chip current is larger than its design value, and the signal levels were less than the usual CMOS values, which may be an artifact of the bidirectional switches, the result shows that the clock recovery on this particular chip works at least in principle.

The pulse width of this recovered clock signal was not enough for processing our computer-generated serial data signal. The minimum pulse width we were able to generate with our computer setup was 2 μs. As discussed above, the logic on the MicroTAG chips assumes that the data is encoded by representing a logic 0 by a 25% duty cycle and a logic 1 by a 75% duty cycle; an example of this is shown in Figure 13. Consequently, the minimum period our signal could have was 8 μs. This means that the recovered clock, with its 1 μs pulse width, was not able to distinguish between the two logic states of the input signal.

Instead, we had to provide the clock signal externally, synchronized with the data signal. In fact, the two signals were generated to be identical, except for the duty cycle, which was a constant 50% for the clock. The data signal consisted of a sequence of 32 "leading" zeros to reset the read control circuit, followed by the actual 16-bit data word; this is shown in Figure 14. The number of leading zeros was doubled from the required value to avoid any possible problem with the reset, caused by the first pulse of any pulse train being wider than the remaining pulses. Though this was not relevant when the clock signal was supplied externally – that signal's first pulse was correspondingly wider itself – it might have caused the recovered clock to misidentify the first bit as a logic 1 and load it and the next 15 bits into the register, rather than resetting the chip.

Sending both the data and the clock to the prototype MicroTAG chip did not lead to the expected results, however. Though the eight data bits to be written to the latch register U5 (Figure 3) alternated between 1 and 0, all outputs of that latch register remained at 0. Suspecting a mismatched chip ID as the reason for this, we measured the on-chip ID to verify if it agreed with the ID bits we were sending. Since it did, excluding this simple explanation for our problem, we decided to postpone further tests until we could obtain better sockets for the chips and concentrate on preparing this proposal which was overdue.

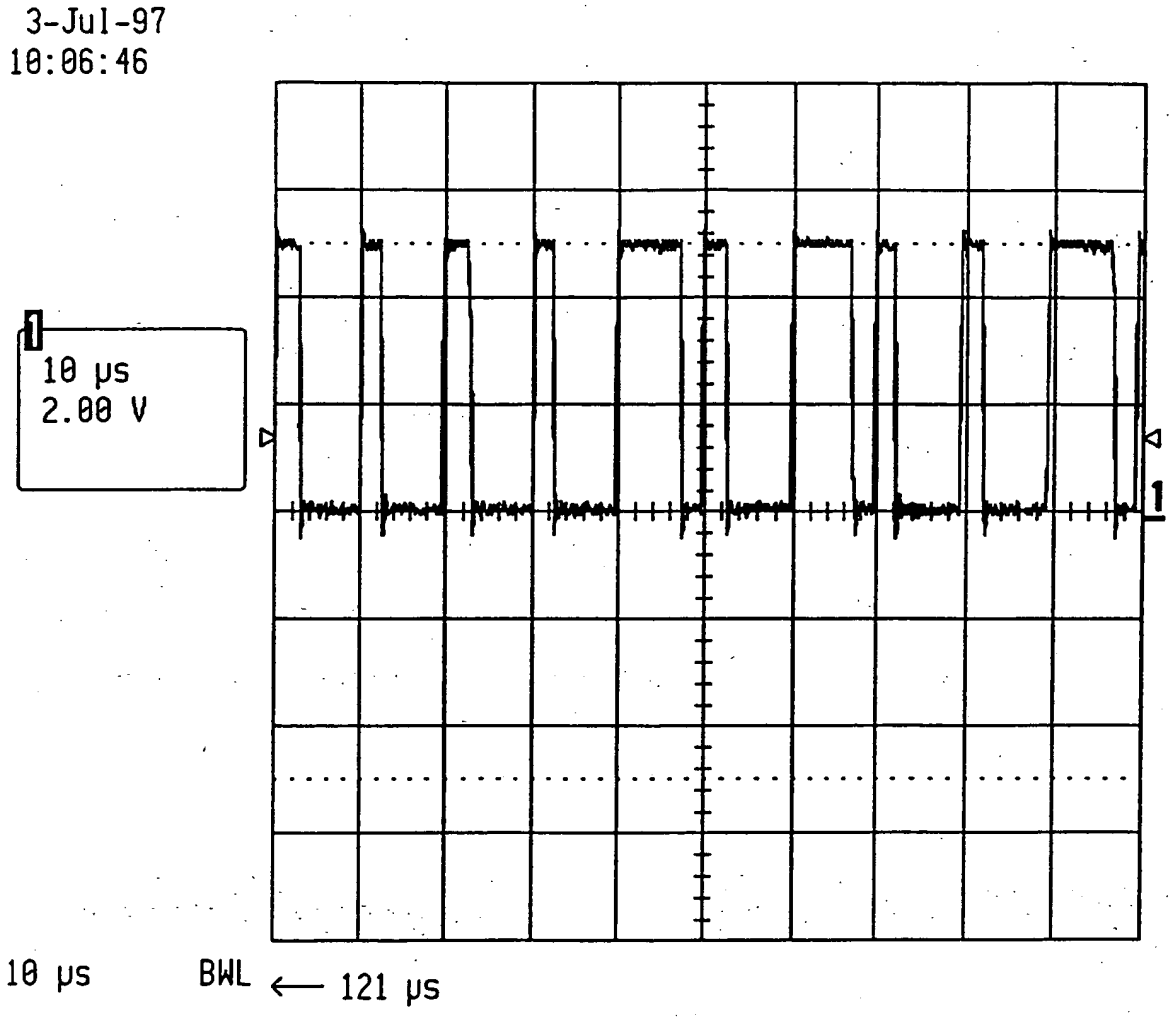

Figure 13: A segment of the computer-generated data signal used to test the MicroTAG chip's read control circuit. The period of the signal is 10 µs. The narrow pulses (≈25% duty cycle) represent logic 0, the wide pulses (≈75% duty cycle) represent logic 1.

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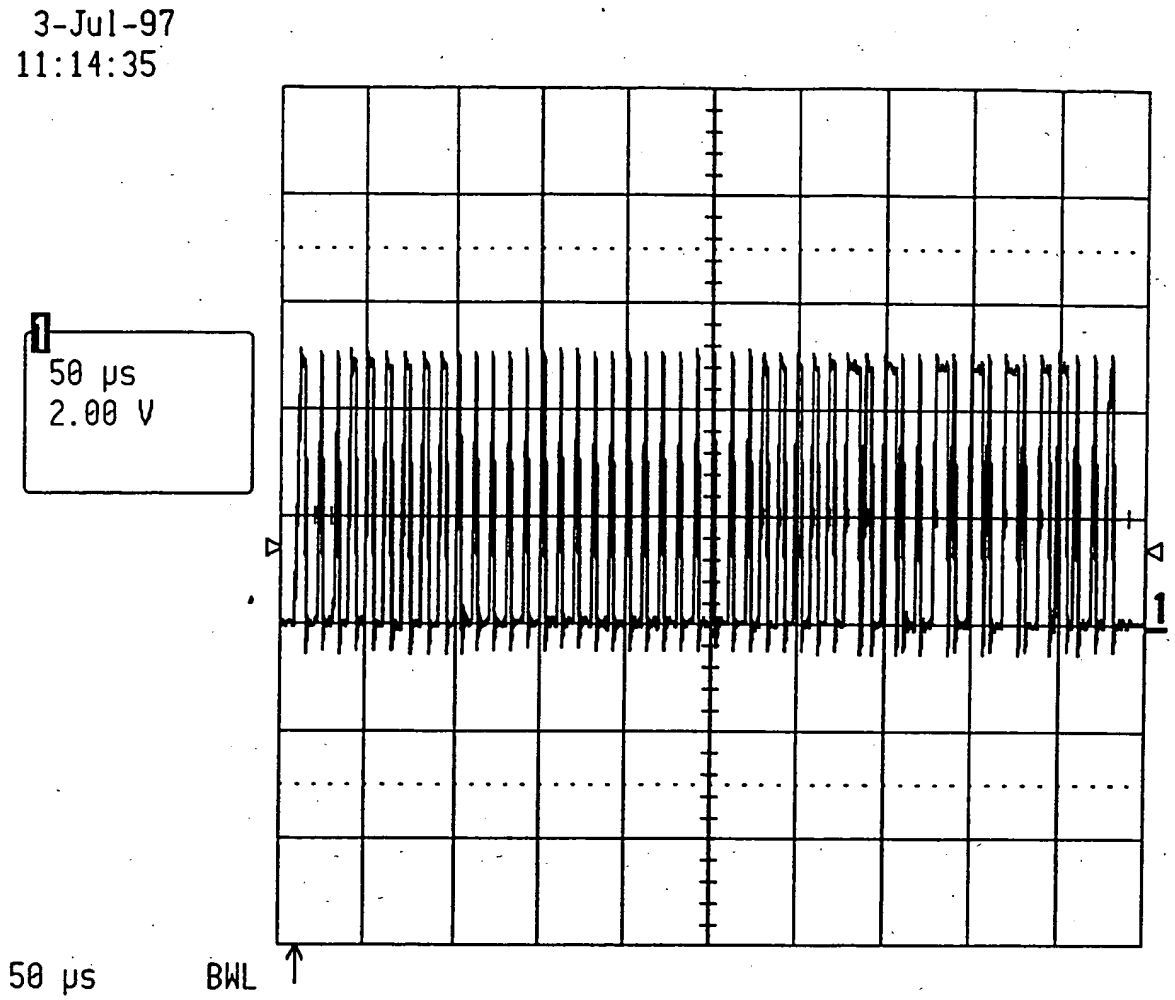

Figure 14: The serial data signal sent to the chip. The pulse train consists of 32 "leading 0s" followed by the actual 16-bit data word.

B. 3 MicroTAG Chip Application System

B. 3. 1 The glue

The glue that is to be used in applying the chip has to fulfill several conditions with respect to application temperature, bond strength, and health hazards:

- The application temperature should be high enough that there is no risk of the glue softening and losing its strength at any of the environmental conditions to be expected once the chip is applied. On the other hand, if the temperature is too high, damage to the chip or the surface of the object being tagged might result, or the glue might solidify before reaching its target.

- The bond provided by the glue has to be strong enough to ensure a reasonable protection against accidental separation of the MicroTAG chip from the package being tagged, e.g., by bumping into other pieces of baggage. Again there is a contradictory requirement, namely that the chip should be removable once it has served its purpose. Considering the wide range of surfaces to be tagged, it appears doubtful that these two requirements can be reconciled completely, short of using one of the following options:

- Using a strong glue and chemical and/or heat treatment to remove it. In view of the large scale of the project, this does not appear to be a realistic option. Also, any such treatment would likely damage some of the materials involved, especially plastics.

- Manually applying the chip, making sure it is in a location where it is protected from accidental contact. Of course, this would defeat the purpose of automating the process as much as possible. One option would be to embed the chip in the paper tag used for routing the baggage – unless the chip is intended to replace the paper tag in the long run.

- Using a strong glue that is not intended to be removed, so the MicroTAG chip would be reusable rather than being discarded each time. This would alter the requirements concerning the long-term reliability of the chip and necessitate an additional component in the application system to identify bags that are already tagged. Finally, this method would likely face problems with public acceptance.

Since none of these alternatives looks realistic, a reasonable compromise will have to be found. With the potential for liability in mind, this compromise will likely have to "err" on the safe side. Note that, of course, these considerations are subject to change when less public projects are concerned, e.g., tagging freight.

– Since the glue will be exposed to large segments of the public, including small children, but also for the protection of personnel working around the MicroTAG applicator, health hazards associated with the glue (and, incidentally, with the chip itself) have to be considered carefully. These hazards include choking, toxicity under various circumstances, such as ingestion, inhalation, or skin contact, burn injuries, and flammability of the material. For these reasons, the glue selected has been used readily and in much larger quantities in general mailing, packaging and other commercial materials for the general public for many years. It is, therefore, safe to use for this application since it has already been in circulation to the general public.

These considerations led to the selection of two types of glue, HM-2703 and HL-2198-X (which is presently qualified as an "experimental product" by the manufacturer), both hot-melt adhesives manufactured by H.B. Fuller Company in St. Paul, MN. The two types are similar to each other in many aspects; the main difference is in their viscosity profile as a function of temperature. The viscosity data from the technical data sheets are summarized in Table I.

Table I: Temperature dependence of the viscosity of the two glue types selected (from the technical data sheets provided by H.B. Fuller Co.).

Temperature		HM-2703 Visc.	HL-2198-X Visc.
(°F)	(°C)	(mPa·s)	(mPa·s)
250	121	137,500	30,000
275	135	35,000	not available
300	149	12,000	4,400
325	153	5,625	not available
350	177	2,750	1,460

The recommended application temperature is 325°F (163°C) for both types. While this may seem like a rather high temperature for some of the plastic materials to be tagged, one has to bear in mind that the heat content of the small drop of adhesive involved (0.2 g or less) is not enough to cause any problems. We verified this by doing a "worst-case test", applying the adhesive to a standard supermarket plastic bag (polyethylene) at a temperature of 190°C (375°F). There was no significant heat-related damage to the bag, at worst a slight wrinkling that might just as well have come from the act of removing the glue in order to inspect the bag. As expected after this, other, less sensitive materials were not affected at all. The materials tested include various kinds of plastics (including those used in hard-shell suitcases), metals, wood, cardboard, paper, leather, glass, and various types of cloth.

With the minor possible exception noted above for plastic bags, removal of the cold glue did not cause any noticeable damage to any of these materials. It should be noted, though, that the clean removal from some of the more textured materials, such as velvet or Velcro, while still not causing any damage, was comparatively difficult to accomplish.

The adhesive strength provided by the glues is not listed in the technical data sheets. Of course, one would expect this parameter to depend on the surface characteristics of the material(s) involved, particularly its roughness. To get an approximate idea about the range of values involved, we performed a series of measurements in the following manner: A block of the material to be tested was clamped down in a vise and a sample of the glue was heated on its surface. Then a plastic (acrylic) disk was pressed into the liquid glue. An eye on the back side of this plastic disk allowed us to insert the hook of a spring balance which we used to measure the force required to break the bond formed by the glue, after it had cooled down and set. This force was then divided by the area of the glue "patty" in order to obtain the strength of the bond. Naturally, this method is limited to materials that can handle the heating process and are either sturdy enough to be clamped down in a vise or heavy enough by themselves to not need any clamping. Moreover, it obviously does not work for any materials that form a stronger bond with the glue than the acrylic itself. Typical values measured were 50–60 kN/m^2 for aluminum, 80–90 kN/m^2 for the surface of a typical hard-shell case, and $\approx$150 kN/m^2 for both wood and acrylic.

One other concern is that at low temperatures the glue might become brittle, possibly reducing its adhesive strength and ability to withstand external forces. Tests done by freezing a test surface after applying the glue showed no noticeable effects of this kind.

The material safety data sheets (MSDS) for both products indicate that there are no known health hazards associated with the cold, solid glue. The potential risks considered in the MSDS include skin contact (no known effects), ingestion (not anticipated to be harmful for amounts up to 5 g/kg of body weight, which should be compared to 0.2 g or less required per chip), chronic effects (none anticipated), effects on other illnesses (none known), and carcinogen status (neither product contains regulated levels of carcinogens listed by various regulatory agencies). There are risks associated with the hot glue, specifically burn risks and irritation of eyes and/or respiratory tract as well as dizziness caused by the vapors. Consequently, the applicators should be located in well-ventilated areas removed from general traffic.

The flash point of the glue is listed as "greater than 400 degrees F" for either material, which is well above the recommended application temperature. This, of course, does not eliminate the need for fire protection devices in case of equipment malfunction.

One risk that is not taken into account in the MSDS, most likely because it is a generic rather than material-specific hazard, is choking. Since the size of our glue pellets falls into the dangerous range – small enough to be swallowed, but large enough to get lodged in a windpipe – this constitutes a risk that definitely has to be considered. The danger is increased due to the fact that the glue is

similar in consistency to gelatin products like gummy bears. It might be reduced, but not entirely eliminated, by adding a suitable substance to embitter the glue. It should be noted that this choking hazard is inherent to the concept of having a small, removable chip on the baggage and is not limited to any particular method of applying the chip nor to any particular kind of glue. The glue used, in fact, is too small to block a windpipe. However, no safe minimum size is defined by authorities. On the other hand, many toys children play with every day such as the eyes or buttons on a doll are, in fact, larger in size than the glue used for MicroTAG application and can be significantly more hazardous.

B. 3. 2 The MicroTAG applicator

During Phase I we developed, fabricated, and tested a manual MicroTAG applicator; its principal components are shown in Figure 15. The system is shown in the position used to insert the glue and chip. The mixing chamber is filled with a chip (simulated in the tests by a 4 X 4 X 1 mm^3 piece of copper) sandwiched between two pieces of glue (each typically 0.1 cm^3 in volume) through the opening in the guide tube. The glue is then heated to the application temperature by the two heating cartridges embedded in the piston on either side of the mixing chamber. As soon as the desired temperature is reached, the piston is moved to the right to align the mixing chamber with the barrel. In practice, since we had no good way to continuously monitor the glue temperature itself but were able to measure the temperature of the heaters, we kept that temperature constant and heated each pellet for a fixed amount of time. Finally, the glue and chip are shot out by a pump-action air gun. The barrel is externally heated by a heat gun, in order to keep the projectiles from cooling down too quickly and getting stuck on their way down the barrel.

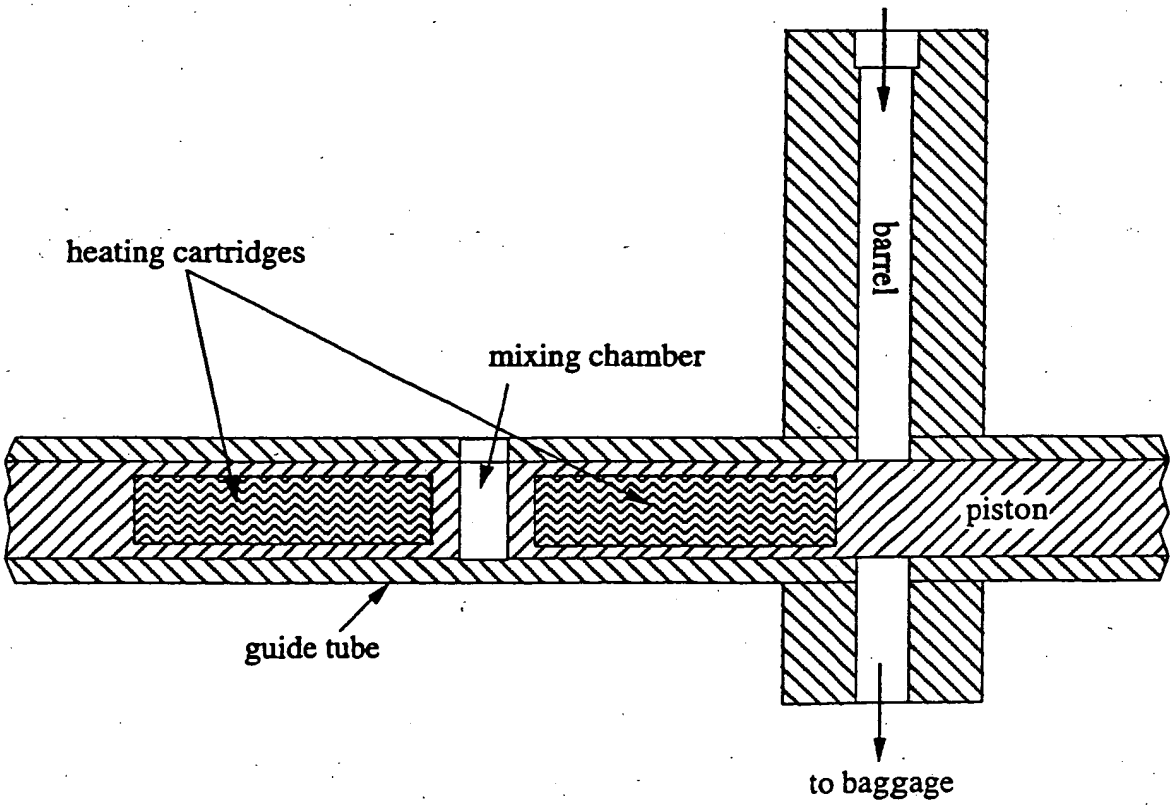

Figure 15: The principal design of the MicroTAG applicator used in the Phase I test.

One problem with this design is that the short, explosive burst of air put out by an air gun makes it relatively difficult to apply just enough force to the chip to get it out but keep it from bouncing off the surface it hits. In our case, this problem was made even more difficult because the control of the air pressure (via the number of times the pump on the gun was used between shots) was rather coarse and led to some variation in the results. While we added a row of small air holes to the upper part of the barrel in an attempt to fine-tune the pressure by covering an appropriate number of them, however due to large pressure variation it was not useful. The air holes did, however serve the additional purpose of providing a safety "valve" in cases where the gun was shot while the barrel was blocked by the piston.

The temperature of the system was monitored by a pair of type J thermocouples that were integrated into the heaters. The calibration of this thermocouple type for the temperature region of interest to us is shown in Table II. There, the temperature of the measurement junction is listed as a function of the thermoelectric voltage between that junction and a reference junction that is kept at 0°C. If the reference junction is at a different temperature, e.g., room temperature, the thermoelectric voltage that corresponds to that temperature has to be added to the measured voltage before determining the measured temperature.

The applicator was tested under various conditions with regard to the amount and the temperature of the glue applied as well as the force with which the glue was shot out (or more precisely, the number of times the pump of the air gun was actuated between shots). The rubbery consistency of the glue and the irregular "pillow" shape in which it was delivered made it difficult to cut it into pieces of a reproducible size. Therefore, we melted the glue and "cast" it in the shape of cylindrical "rods" 4.75 mm in diameter, after running a series of tests to verify that repeated heating and reheating of the glue did not noticeably degrade its performance. These rods were then cut to the desired length, between 3 and 7 mm, which corresponds to volumes between 0.05 and 0.12 cm^3. The advantage of this method was that the uncertainty in the amount of glue was due to just one cut over a relatively small area; that cut was much easier to control than the ones needed to "carve" the required amount out of the original pillow.

The dependence of the efficiency of the manual MicroTAG application system on the amount of glue used is shown in Table III and Table IV. The difference between the two tables is the amount of force used to shoot out the glue and chips. The data in Table III were obtained by pumping the air gun once between successive shots; in Table IV we pumped twice between shots. In both cases, the system was kept at a temperature of 160°C. This was slightly above the recommended application temperature, to compensate for the fact that the measurement was made directly at the heater rather than in the mixing chamber. The heaters were regulated to keep the readout of the thermoelectric voltage within ±0.1 mV of the nominal value; this corresponds to a temperature variation of ±2°C. For each shot, the applicator was filled with a copper test chip sandwiched between two pieces of glue each of which had half the size specified in the table. Once the filling was completed, the glue and chip were left in the applicator for 15 s, in order to melt the glue, and then shot out onto a hard-shell briefcase used as a test target. This was done 20 times for each condition.

Table III clearly indicates that pumping the air gun once is not sufficient to reliably get the glue and chip shot out of the applicator. In more than half the attempts, the glue and chip did not come out of the air gun barrel, regardless of the amount of glue used. In fact, when we used 0.24 cm^3 of glue, the result was so consistent that we decided to give up after ten attempts. When pumping twice (Table IV), the situation changed significantly. In this case, the force was sufficient to get the projectile out most of the time, but now we had an increased risk of seeing the chip bounce off the surface of the target, at least for the two smaller sizes. For the 0.24 cm^3 samples, the number of chips bouncing off was minor; here, the large amount of glue helped cushion the chip's impact on the surface. Due to the limited size of the mixing chamber, we were not able to investigate whether the improvement in our success rate continued for even larger amounts of glue. However, we expect

to be able to use less glue with the automatic applicator we propose for Phase II, when we will have a more accurate control over the air pressure applied to the chip. The lack of reproducibility of the air gun is reflected in the fact that we had chips both bouncing off the target and getting stuck in the barrel under the same conditions. Of course, some of this effect may very well be due to variations in other parameters, such as the orientation of the chip with respect to the axis of the gun barrel or the precise amount of glue used. To account for these variations, an adaptive control of the air flow may be necessary in the automatic version of the applicator.

Table II: Calibration of type J thermocouples (R.L. Powell et al., 1974). The temperature T of the measurement junction is listed as a function of the thermoelectric voltage U between that junction and a reference junction that is kept at 0°C.

U (mV)	T(°C)	U (mV)	T(°C)	U (mV)	T(°C)	U (mV)	T(°C)
0.0	0.0	2.5	48.4	5.0	95.1	7.5	140.8
0.1	2.0	2.6	50.3	5.1	96.9	7.6	142.6
0.2	3.9	2.7	52.2	5.2	98.8	7.7	144.4
0.3	5.9	2.8	54.1	5.3	100.6	7.8	146.2
0.4	7.9	2.9	56.0	5.4	102.4	7.9	148.0
0.5	9.9	3.0	57.8	5.5	104.3	8.0	149.8
0.6	11.8	3.1	59.7	5.6	106.1	8.1	151.6
0.7	13.8	3.2	61.6	5.7	108.0	8.2	153.4
0.8	15.7	3.3	63.5	5.8	109.8	8.3	155.2
0.9	17.7	3.4	65.4	5.9	111.6	8.4	157.0
1.0	19.6	3.5	67.2	6.0	113.4	8.5	158.9
1.1	21.6	3.6	69.1	6.1	115.3	8.6	160.7
1.2	23.5	3.7	71.0	6.2	117.1	8.7	162.5
1.3	25.4	3.8	72.8	6.3	118.9	8.8	164.3
1.4	27.4	3.9	74.7	6.4	120.8	8.9	166.1
1.5	29.3	4.0	76.6	6.5	122.6	9.0	168.0
1.6	31.2	4.1	78.4	6.6	124.4	9.1	169.8
1.7	33.1	4.2	80.3	6.7	126.2	9.2	171.6
1.8	35.1	4.3	82.1	6.8	128.1	9.3	173.4
1.9	37.0	4.4	84.0	6.9	129.9	9.4	175.2
2.0	38.9	4.5	85.8	7.0	131.7	9.5	177.0
2.1	40.8	4.6	87.7	7.1	133.5	9.6	178.8
2.2	42.7	4.7	89.5	7.2	135.3	9.7	180.6
2.3	44.6	4.8	91.4	7.3	137.2	9.8	182.4
2.4	46.5	4.9	93.2	7.4	139.0	9.9	184.2

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Table III: The efficiency of the Phase I MicroTAG applicator as a function of the amount of glue used. The air gun was pumped once between successive shots.

	Number of chips		
Amount of glue (cm^3)	sticking to target	not out of barrel	bouncing off target
0.10	7	11	2
0.18	7	11	2
0.24	0	10	0

Table IV: The efficiency of the Phase I MicroTAG applicator as a function of the amount of glue used. The air gun was pumped twice between successive shots.

	Number of chips		
Amount of glue (cm^3)	sticking to target	not out of barrel	bouncing off target
0.10	9	4	7
0.18	12	1	7
0.24	15	3	2

Next, we extended the tests for the large (0.24 cm^3) sample to larger forces, pumping the air gun three times between successive shots. The result is shown in Table V, together with the corresponding results for one and two pumps. The marked increase in the number of chips bouncing off the target makes it obvious that the force obtained from pumping the air gun three times is too much for our purposes.

Finally, we tested the system as a function of the heater temperature. Using the optimal conditions determined in the previous measurements (0.24 cm^3 of glue, two pumps of the air gun), we performed two additional series of test shots with a temperature of 142°C and 178°C respectively (the odd numbers are the result of changing the thermoelectric voltage measured by ±1 mV relative to the previous setting). The results for these tests are shown in Table VI, together with those for 160°C. Increasing and decreasing the temperature both led to a deterioration in the performance of the applicator. This can be understood by considering the viscosity of the glue as a function of temperature (cf. Table I above). At low temperature, the viscosity increases rapidly, making it more difficult to form a good bond between the glue and the chip in the time available (which was kept unchanged, at 15 s, throughout the three test series), negating the cushioning effect of the glue discussed above. In fact, at 142°C we frequently observed that the two pieces of glue came out separately, from each other and the chip, and were still recognizable as small cylinders. The higher viscosity and resulting lower adhesiveness of the glue also explain why no samples got stuck in the barrel at this temperature.

At 178°C, on the other hand, the viscosity of the glue was already so low that it tended to be blown off the chip and come out as a rather widely distributed "spray". Of course, this again made the glue unavailable as a "shock absorber". The results show that an accurate temperature control will be important for a reliable operation of the MicroTAG applicator.

Table V: The efficiency of the Phase I MicroTAG applicator as a function of the force applied in shooting out the glue and chip. This force is expressed in terms of the number of times the pump of the air gun was actuated between successive shots. The amount of glue used was 0.24 cm^3.

	Number of chips		
Number of times air gun was pumped	sticking to target	not out of barrel	bouncing off target
1	0	10	0
2	15	3	2
3	9	0	11

Table VI: The efficiency of the Phase I MicroTAG applicator as a function of the heater temperature. The amount of glue used was 0.24 cm^3; the air gun was pumped twice between successive shots.

	Number of chips		
Temperature (°C)	sticking to target	not out of barrel	bouncing off target
142	8	0	12
160	15	3	2
178	10	4	6

In summary, we have been able to reach an efficiency of 75% in applying our test chips to the test surface. In view of the known shortcomings of the design (such as the use of a low-cost off-the-shelf air gun), which were caused by Phase I budget limitation due to the high cost of the prototype MicroTAG chip layout and fabrication and time constraints, we expect to increase the efficiency significantly for the proposed Phase II version of the applicator. Therefore, once the new automatic MicroTAG applicator is developed during Phase II we expect to be able to optimize the applicator to approach 100% efficiency. A photograph of a copper chip embedded in the glue and applied onto a suitcase surface is shown in Figure 16.

B. 4 References

Powell, R.L., et al., "Thermocouple reference tables based on the IPTS-68" NBS monograph 125, 1974.

Figure 16: Photograph of one of the copper chips used to test the chip applicator, after its application

C PHASE II TECHNICAL OBJECTIVES AND APPROACH

C. 1 Phase II Objectives

During Phase II, the design of the prototype MicroTAG chip developed will be tested further in detail, characterized, and optimized. A second fully functional prototype will be manufactured. According to the results of the second prototype, a final candidate MicroTAG chip will be designed and a sufficient number of tags, which may be used with the prototype ABIS system or other projects, will be manufactured, tested, and delivered to DoD/Army.

A prototype remote programmer/reader will be also designed, manufactured, and tested for interrogating *NOVA*'s MicroTAG chips. The prototype remote programmer/reader manufactured will be delivered to DoD/Army together with the tags.

The manual MicroTAG applicator system developed during Phase I will be converted into an automatic tag application system. It will be designed, optimized, manufactured, and tested during Phase II. The applicator will be also delivered to *DoD/Army* at the end of Phase II for incorporation into the prototype ABIS system under development at *NOVA* and *ARDEC* or other projects.

C. 2 Phase II Tasks

The tasks of the proposed Phase II program are given below:

Task 1. Test, characterize, and optimize prototype MicroTAG chip developed during Phase I.

Task 2. Design and fabricate a fully functional second prototype MicroTAG chip.

Task 3. Test and characterize the second prototype MicroTAG chip.

Task 4. Improve the design and fabricate a fully functional final candidate prototype MicroTAG chip.

Task 5. Test and characterize the final candidate prototype MicroTAG chip.

Task 6. Design and build a prototype remote programmer/reader for the MicroTAG chip.

Task 7. Test and evaluate the prototype remote programmer/reader for the MicroTAG chip using prototype MicroTAG chips if applicable.

Task 8. Design and simulate a remote programmer/reader using the test results.

Task 9. Fabricate the final candidate prototype remote programmer/reader for the MicroTAG chip.

Task 10. Test, characterize, and calibrate the final candidate prototype remote programmer/reader using prototype MicroTAG chips.

Task 11. Design and manufacture a prototype automated version of the manual MicroTAG applicator developed during Phase I.

Task 12. Test and evaluate the prototype automatic MicroTAG applicator, verifying the performance of the glue selected in the Phase I study for use with the new applicator in the process.

Task 13. Improve, modify, and optimize the prototype automatic MicroTAG applicator.

Task 14. Test and calibrate the prototype automatic MicroTAG applicator.

Task 15. Integrate the prototype MicroTAG applicator into *NOVA*'s prototype ABIS baggage inspection system, if needed.

Task 16. Evaluate and optimize the integrated MicroTAG applicator and baggage inspection system.

Task 17. Deliver the prototype MicroTAG applicator and remote programmer/reader with prototype MicroTAG chips to *ARDEC.*

Task 18. Train the *ARDEC* personnel on the use and application of the prototype MicroTAG, remote programmer/reader, and MicroTAG applicator.

Task 19. Prepare the final design documents of the MicroTAG chip, MicroTAG applicator, and the remote programmer/reader for commercialization during Phase III.

Task 20. Present and demonstrate the Phase II results to *DoD/Army* officials at important milestones.

Task 21. Write Phase II Final Report.

C. 3 Phase II Task Schedule

Work will start immediately on Task 1. Most of this task will be accomplished before the formal start of Phase II, in the course of finalizing the Phase I results. In the time line of Phase II, this work is expected to take less than one month. The design and layout of the second prototype MicroTAG chip (Task 2) can also start immediately, parallel to Task 1. This is expected to take five months, plus two months for the actual chip fabrication. As soon as the chip layout is finished, work can begin on a test system, which will allow us to start testing the second prototype MicroTAG chip (Task 3) immediately after it is delivered by the foundry. The results from these tests, which are expected to take about two months, can then be incorporated into the design of the third and final prototype MicroTAG chip (Task 4). We anticipate that this task, which also includes the fabrication of the chip, will require about six months. Since this final prototype chip will not have any test pads, it will have to be tested using the remote programmer/reader (cf. Task 6 to Task 10). Those tests (Task 5) are expected to take about two months. One of the aspects of these final tests will be to apply some of the chips to pieces of baggage (or equivalent test surfaces), using the applicator discussed below, and verify that this treatment has no significant detrimental effect on the performance of the chips.

The design of a first prototype remote programmer/reader (Task 6) will of course have to take into account the data transfer protocols that the then-current chip design uses, both for transmission to and from the chip. While there may be significant differences in that respect between the first and second prototype versions of the chip, we anticipate at most minor adjustments after that. Consequently, Task 6 should proceed concurrently with Task 2, the design and layout of the second prototype MicroTAG chip. Tests of this programmer/reader (Task 7)will be performed at the same time as Task 3 and will possibly extend one half to one month beyond the completion of that task. Similarly, the final prototype of the programmer/reader will be designed (Task 8) and fabricated (Task 9) in parallel with the corresponding tasks for the final chip prototype, and the two will be tested together (Task 5, Task 10).

The experience gained with the manual MicroTAG applicator that was developed during Phase I (cf. section B. 3. 2) will enable us to develop an automated prototype in a relatively straightforward manner; the general concept for this will be discussed below in section D. 5. We expect this development and the actual fabrication of a prototype (Task 11) to require approximately six months. For the ensuing tests of the system, using the glue selected in Phase I, we anticipate about two months (Task 12). The results of these tests will then be used to improve and optimize the applicator (Task 13). The extent of the changes required will determine whether we can modify the existing setup or have to build a second model. In the latter (worst) case, the task is estimated to require four months to complete. The final tests of the modified applicator (Task 14) are expected to take about two months. Finally, we expect to be able to integrate the applicator into the Baggage inspection system being developed at *NOVA* and test the integrated system in three and two months respectively.

The proposed task schedule for Phase II is shown in the time-line chart in Figure 17, grouped according to the three principal components of the system. As this chart indicates, the schedule leaves reserves for unforeseen delays in each group.

Figure 17: Time-line chart for Phase II tasks .

D PHASE II WORK PLAN

D. 1 Introduction

In this section the development of the three parts of the Phase II project, namely MicroTAG chip, remote programmer/reader, and MicroTAG chip applicator will be discussed. The main emphasis will be placed on the MicroTAG electronics which is, by itself, the most important and difficult component of the whole system.

Most of the work will be carried out at *NOVA* until the developed prototype MicroTAG chip, remote programmer/reader, and MicroTAG chip applicator are delivered to *ARDEC* at the end of the Phase II work. The silicon layout of the MicroTAG chip will be contracted out. The cost for this is expected to be less than 10% of the total Phase II funding.

D. 2 Phase II General Plan

During Phase II the design of the MicroTAG chip will be improved and optimized using the Phase I results. A second prototype will be manufactured. According to the results of the second prototype the final MicroTAG electronic circuit will be designed and a sufficient number of tags will be manufactured for delivery to DoD/Army.

A prototype remote programmer/reader will also be designed and developed using the Phase I investigation results. The prototype manufactured will be delivered to DoD/Army together with the tags.

The applicator system will also be finalized during Phase II using the results obtained in Phase I. A prototype applicator will be developed during Phase II. The applicator will also be delivered to DoD/Army at the end of Phase II.

D. 3 The Smart MicroTAG Chip

The first prototype smart MicroTAG chip developed during Phase I work will be tested further during Phase II study. The size of the new prototype tag chip to be developed during Phase II will be smaller than the present prototype size, $4 \times 4 \times 0.3$ mm^3. The planned size is $3 \times 3 \times 0.1$ mm^3. The MicroTAG chip is designed to be completely self-contained. The prototype chip designed and fabricated during this project will contain connection pads for testing. The final chip to be manufactured at the end of Phase II will not contain any connections pads to minimize its size. The new prototype MicroTAG chips developed during Phase II will contain two antennas placed on opposite sides of the chip similar to the first prototype described above. One of them receives the microwave signal from the interrogator which is used for both to power the chip by storing charge onto a large on-chip capacitance bank and to transmit data to the chip. The second antenna is used to transmit the chip's response to any data requests from the interrogator. Rather than using an (power-intensive) active transmitter for this purpose, this antenna is set up in the Phase I design to reflect a continuous wave from the interrogator with varying efficiency; the data from the chip is encoded in the pattern of the efficiency variation. For details of this "modulated backscatter" design see the discussion in section B. 2. For the Phase II design we plan to use the same principle, although we will likely have to add spread-spectrum techniques in the final design to increase the noise immunity of the system.

The MicroTAG chip fabrication process to be used for the final product is expected to be about 0.25 to 0.8 micron to achieve small size and low power design. For example, a 0.25 micron process requires only 1.8 V for the digital circuitry. However, the Phase I prototypes were manufactured using a 1.2 micron process. Initial Phase II prototypes may also be manufactured using a larger minimum line width process such as 1.2, 0.8 or 0.5 micron.

A computer aided design (CAD) program developed for modeling and simulating electromagnetic devices used during Phase I is also expected to be used during Phase II. This program is especially useful to design, simulate, and optimize the receiving and transmission antennas. In this work the

spacing and thickness of the antenna metal will be optimized for application to the proposed smart MicroTAG chip. The test results obtained from the first prototype version will be used during Phase II to fully optimize the MicroTAG chip design.

The external remote programmer/reader will send out radio frequency power to the antenna on the chip. The received power will be used to charge up a capacitor. The output of the capacitor will then be used to power the chip. The rest of the circuit on the chip will be low power CMOS circuits that will receive the signal from the remote programmer/reader and store the information in the non-volatile memory. If a read request comes from the programmer/reader, the chip will also have the functionality to transmit the contents of the memory through the antenna. Details of the digital circuitry are discussed in section B. 2 above.

Other functions such as having a unique MicroTAG number for identification of which MicroTAG is programmed or read out will also be studied and implemented if required. Such a unique identification number can be important if there is more than one MicroTAG inside the aperture field of the remote programmer/reader.

The cost of the chip will be kept as low as possible by using small die size on large 6", 8" or 12" wafers. For example, from a single 8" wafer we expect to get approximately 10,000 2 x 2 mm^2, 3,000 3 x 3 mm^2, and 2,000 4 x 4 mm^2 dies. Small dies with relatively simple circuitry may have exceptionally high yield reaching up to 80%. In large quantities each wafer is expected to cost much less than $400 to process. This shows that even with 50% yield at $400 per wafer and for the largest die size considered, i.e., in a worst-case scenario, the fabrication cost of the tags is no more than 40 cents per chip. If the smallest die size is used then the cost can be easily few cents per die. Recently 12" wafers are becoming available which can reduce the cost even further. The cost of the initial prototypes will be much higher due to the low numbers required and the large non-recurring engineering cost which includes the design, layout, simulations and the mask set.

A second factor involved in the cost is the selection of the working tags for deployment. Since the production tags will be completely self-contained, the testing will not require a probe card and a costly probe station. The dies can be placed onto a conveyor belt passing in front of a test and selection system. The test system will be similar in design to the remote programmer/reader unit. It will be programmed to power the tag, write and read several coded data to test and select the working chips. These tests can be fully automated, further reducing the cost. Such a quality control system can be built at *NOVA* during Phase III. It may also program a unique ID number onto the MicroTAG chip if required. In fact, the complexity of the chip and hence the cost of the system could be reduced significantly by limiting the information stored on the chip to this unique ID number and storing all other relevant data associated with that ID on a stationary computer system connected to the interrogator. As an added benefit, this simplified solution would greatly reduce potential problems stemming from unauthorized access to the data on discarded chips; without simultaneous access to the "stationary" data, the ID numbers on the chips would be meaningless. On the down side, this solution would require a bigger range of ID numbers, since those numbers would now have to distinguish all the records stored in the computer system at any given time, rather than just minimizing the chance of having two chips with the same ID in the field of view of an interrogator.

Some aspects of the proposed MicroTAG chip design were too complex for a full investigation within the scope of Phase I. One option that will be studied in more detail is to use GaAs rather than CMOS technology. This would definitely improve the chip's microwave capabilities, but it remains to be investigated whether these improvements justify the increased cost. Other issues that will be resolved during Phase II are discussed in the following subsections.

D. 3. 1 Antenna Circuit for the Smart MicroTAG

One of the most important section of the proposed MicroTAG chip is the antenna circuit. It will be designed to receive the maximum possible power from the remote programmer/reader and store it onto a capacitor for use by the MicroTAG chip for receiving signals, decoding and storing the data into memory, and transmitting data back to the remote reader. In the current chip design (Phase I), it

is executed as a simple patch antenna. Other antenna types such as dipole, half wave, quarter wave, etc. will be carefully studied and simulated. Each antenna type has its own benefits and problems. The simulations will help the selection of the best antenna type for the proposed system.

Alternatively, the receiver circuit may be formed from a closed loop antenna with several turns running around the perimeter of the integrated circuit. The antenna will be attached to a parallel LC tank circuit (Figure 18). This circuit forms its highest impedance at the resonant frequency of the LC tank circuit so the transmission/receiver wavelength will be set to this frequency.

Antenna placement onto the MicroTAG chip may have a lot of potential problems that must be avoided. One of these is the width of the antenna line. It must be carefully optimized as the adjacent layers can be electrically shorted to form a single line. The thickness and width of the antenna line should also be kept as large as possible. Since the aim is also to produce the smallest chip area, a compromise must be made that will work. Three dimensional simulations of the antenna system will be used to accomplish this.

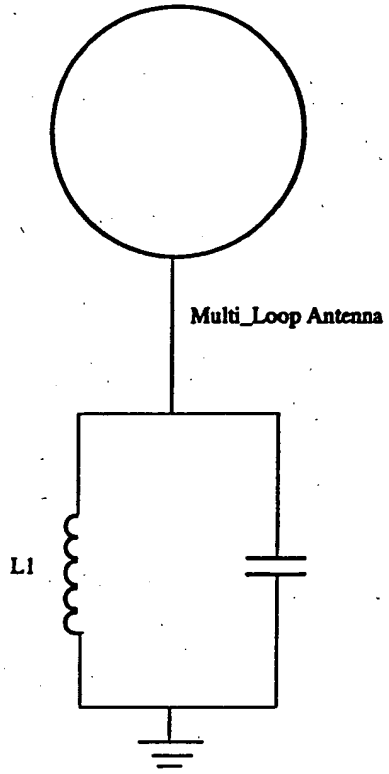

Figure 18: Parallel tuned antenna circuit.

The efficiency of a loop antenna is related to the loop radius as the fourth power and the induced current squared as given in the formula below.

D. 3. 2 Transmitting through a Small Circuit Loop Antenna

The power radiated from a loop antenna can be obtained (Ramo, Whinnery and Van Duzer, 1965) by integrating the time averaged Poynting vector,

$$\bar{P} = \bar{E} \times \bar{H},$$

which is the power density at any point. In spherical coordinates, the total power radiated is

$$W = \int_0^{\pi} \int_0^{2\pi} P_r r^2 \sin\theta d\theta d\phi = \int_0^{\pi} \int_0^{2\pi} K \sin\theta d\theta d\phi,$$

where P_r is the radial component of the Poynting vector and K is defined as the radiation intensity. For a loop antenna, K is obtained as

$$K = \frac{\eta}{8\lambda^2} k^2 \pi^2 a^4 I^2 \sin^2\theta = \frac{\eta}{32} (ka)^4 I^2 \sin^2\theta .$$

The power radiated by the loop antenna is

$$W = 2\pi \int K \sin\theta d\theta = \frac{\pi\eta}{12} (ka)^4 I^2, \qquad (1)$$

where a is the radius of the loop, η comes from the impedance of media, and k is the wave constant.

D. 3. 3 EEPROM Memory Organization

The EEPROM memory is organized to read and write under the address control. A single cell of a core memory is shown in Figure 19. The EEPROM cells are MOSFETs with the extra floating gate controlled by the ROW LINE. In write operation the appropriate column is selected by the column multiplexer. After selection the row line is pulsed to erase all the cells to zero. A one can be written to the appropriate cell by selection of the row select line. The high voltage switch is enabled and a high level signal is applied to the drain of the MOSFET selected for write. The high voltage can be generated by a circuit similar to the one shown in Figure 8. The MOSFET stores a one when it is selected. In read operation the cell is addressed by the row and column registers. Each column will be high corresponding to a stored zero and low corresponding to a stored one. The sense amplifier and logic creates the correct output sense for positive logic.

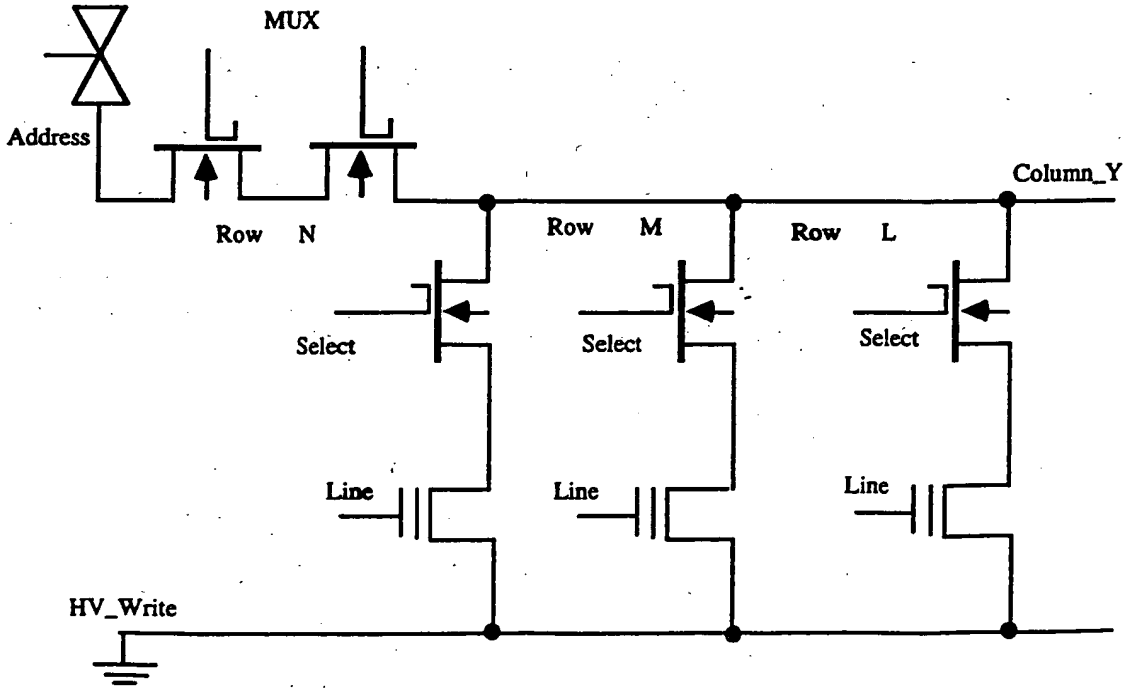

Figure 19: The EEPROM memory circuit (only one cell is shown).

D. 4 MicroTAG Chip Remote Programmer/Reader

The remote programmer/reader for the MicroTAG chip will have to perform three basic tasks:

1. Power up the chip by transmitting microwave power to it which, after rectification, will be stored on the on-chip capacitor array to provide a constant supply for the duration of the data exchange between chip and interrogator.
2. Transmit data to the chip. These data can either contain information to be written to the on-chip memory or consist of a request to the chip to transmit all or part of its memory contents back to the interrogator.
3. Receive data from the chip. With the current concept for data transmission from the chip, this task will consist of two parts, sending out a carrier wave and receiving the modulated backscatter of that wave.

Any transmission to or from the chip will require high frequency microwaves to achieve an acceptable degree of efficiency, due to the small size of the MicroTAG chip and of any antennas that can be placed on it. While the current chip design was made for a frequency of 10 GHz, we may use slightly higher frequencies in the final version of the MicroTAG chip.

The current concept for data transmission to the chip calls for a frequency modulation of the carrier wave with one of two frequencies, with the pattern of the modulation representing the data to be transmitted. The principal design of a transmitter that could generate such a signal is straightforward; it is shown in Figure 20. A digital circuit produces the pattern to be transmitted, which, at this stage, is represented by two different voltage levels. These levels are used to tune a voltage-controlled oscillator whose output is amplified and transmitted to the chip through a suitable antenna. We will continue to study alternatives to this transmission concept with respect to efficiency, reliability (mainly noise immunity), and ease of implementing the corresponding receiver on the MicroTAG chip.

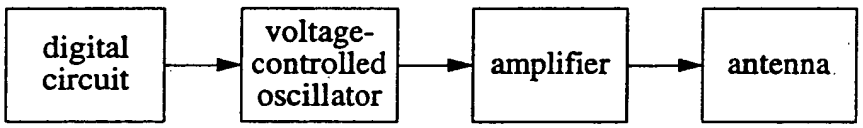

Figure 20: Block diagram of a circuit for frequency-modulated data transmission.

When transmitting data from the chip to the interrogator, the information will again be encoded in a pattern formed by modulating the carrier wave with two different frequencies. In this case, our present concept, realized in the Phase-I version of the MicroTAG circuit, calls for chopping the reflected wave with the respective frequency. On the receiver side, the incoming signal will then be sent through a filter that detects only the slow variation of the signal, but not the high carrier frequency. This will be followed by a pair of high- and low-pass filters, tuned midway between the two modulation frequencies, and suitable logic circuitry to decode the pattern sent by the chip.

Special attention will have to be paid to the design of the antennas used by the interrogator to transmit and receive data and power, particularly their directional characteristics. On one hand, we want the transmission to be as efficient as possible, which would imply a strongly focussed beam. On the other hand, the position of the chip passing by the programmer/reader is not known a priori, so the system's aperture has to be large enough to guarantee that the communication can be established. Obviously, a compromise will have to be found between these two conflicting requirements.

In summary, the remote programmer/reader will produce microwaves tuned to the MicroTAG antenna for transferring power to the chip. It will also transmit data and/or an identification number to the MicroTAG chip. The identification number can be already programmed into the MicroTAG chip before application. The remote programmer/reader will also have the capability to ask the chip to send its memory contents and be able to read the data transmitted by the tag. Each cycle: send power, send data or request for data to tag, and read tag, will be done sequentially.

The cost of the remote programmer/reader will largely depend on the microwave power required and, to a lesser degree, on the frequency we will use. Another important factor is whether it will be possible to use the same transmitter both for the actual data transmission to the chip and to generate the carrier wave for the modulated backscatter, or whether we will have to use separate devices for the two tasks. Consequently, it is difficult to give a reliable estimate for the eventual production cost of this device, but we may reasonably expect production costs to be below $3,000.

D. 5 MicroTAG Chip Applicator

The requirements for the applicator are extensive, as described in section A. 1. We propose a simple but novel technique to meet these requirements. The proposed applicator will be made of a simple glue gun. A jelly type of glue that does not harden but retains its adhesive quality for a long period of time measured in days will be used; a suitable candidate has been identified during Phase I (cf. section B. 3. 1). The tags will be embedded into the glue, and glue balls containing a MicroTAG chip will be propelled onto a piece of baggage. The diameter of the glue ball will be between 3 and 5 mm. This type of glue practically attaches itself to any known material. The only problematic surfaces may be oily surfaces and possibly teflon. Please note that the MicroTAG can be used with other type of applicators or without an applicator placed in any type of environment.

The process of applying a MicroTAG chip to a given piece of baggage can be broken up into several steps:

1. Melt the glue and insert it into the mixing chamber. For an automated system, this is likely to be the order required to guarantee that the same amount of glue is used each time. Apart from this consideration, though, there is nothing that would require this particular order of events, rather than melting the glue only after it reaches the mixing chamber. This latter method might in fact be advantageous if it is intended to use prefabricated glue-chip pellets, instead of mixing the two components in situ as discussed in step 2.
2. Insert the chip into the mixing chamber with the liquid glue. The glue temperature should be adjusted such that its viscosity allows the chip to sink to the center of the drop of glue in the time available. This will result in the best chance for the chip to stay with the glue during the shooting process. Alternatively, the same goal can be achieved by inserting the chip between two layers of glue with correspondingly higher viscosity. A relatively high viscosity also helps ensure that the glue is not "blown off" the chip by the air used to shoot the glue-chip combination onto the baggage.
3. Move the glue-chip combination to the barrel of the air "gun" used to shoot it out. There are two reasons why this is more advantageous than mixing glue and chip directly in the barrel. The first is that depending on various parameters the time required to heat the glue and bring it in good contact with the chip may be longer than the separation between successive pieces of baggage. In this case using several mixing chambers that successively move into the same barrel will be easier and more economical than having several barrels, each with its own valves and feeding system for glue and chips. Secondly, moving the glue-chip pellet into the barrel just in time prevents it from dropping out prematurely under its own weight.
4. Shoot the glue-chip pellet onto the object passing by under the barrel. While we use the term "shoot" here, our Phase-I tests (discussed above) indicate that this is not the optimal way to propel the chip onto its target. "Shooting" implies a short, explosive burst of air; that makes it hard to keep the proper balance between applying enough force to get the pellet out of the barrel

and avoiding to shoot it out so violently that the chip bounces off the surface it hits. A longer-lasting, continuous, and preferably adjustable stream of air is expected to lead to a significantly better performance in this respect.

5. Design a system to remove any glue residue from the barrel to keep the system from clogging up and avoid uncontrolled dripping of glue.

These steps are realized in the conceptual design shown in Figure 21. The glue is stored in a tank, from where it flows through a suitable valve into a mixing chamber. It remains to be investigated whether an active pump mechanism is needed in order to accomplish this. The chips can either be transported to the mixing chamber by a tape conveyor system, similar to those used for transporting surface-mount components, or be stored in a container above the mixing chamber, with a suitable mechanism to reliably get out individual chips. The latter option is shown in Figure 21. The filled mixing chamber then moves on to the right, towards the barrel of the air gun. When the chamber with the glue-chip pellet reaches the barrel and a piece of baggage arrives below it, the air valve opens just long enough for the air stream to flush out the projectile onto the target. After each "shot" the barrel will have to be cleaned from glue residue to avoid clogging and accidental spillage. The cleaning rod indicated in Figure 21, which would move down the barrel to scrape the glue off the walls is only one of the options we are considering; details will have to be investigated during Phase II of the project. One important element of the MicroTAG applicator that is not shown in Figure 21 is the heating system. Any part of the applicator that can come in contact with the glue will have to be heated to the correct application temperature to keep the pellets from sticking to the walls. It remains to be investigated in Phase II whether preheating the pressurized air will lead to a big enough improvement in the system's performance to justify this measure.

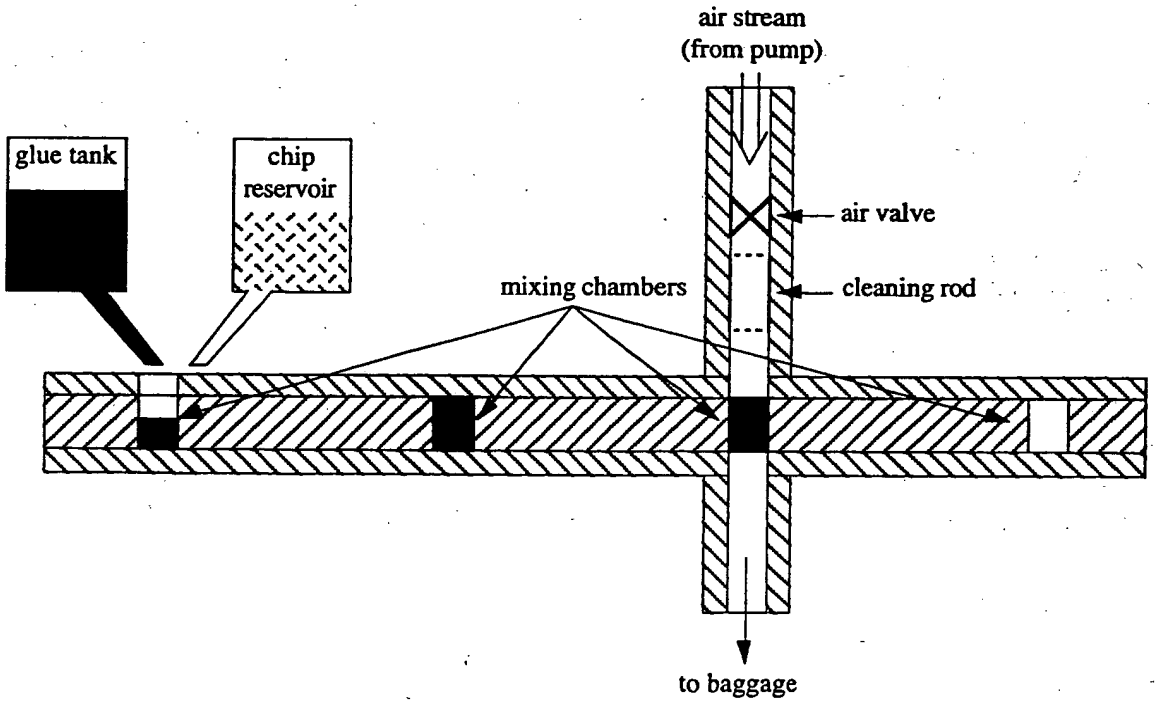

Figure 21: Conceptual design of the MicroTAG applicator (not to scale).

D. 6 Integrating the MicroTAG Chip Applicator into *NOVA*'s Automated Baggage Inspection System (ABIS)

If it is intended to tag only those baggage items which trigger a baggage inspection system, for example the ABIS system currently being developed at *NOVA*, and *ARDEC* it will be necessary to

integrate both the MicroTAG applicator and a remote programmer/reader into that system. To achieve this, we plan to place a MicroTAG applicator on the same conveyor belt as the ABIS inspection system, down the line from the latter. This is shown schematically in Figure 22. Upon detection of suspicious items, the ABIS system will send a signal to the MicroTAG applicator, causing it to shoot a MicroTAG chip onto the piece of baggage in question. The distance between the x-ray system and the applicator will obviously depend on the time it takes to reach a decision and prepare the chip for application, and on the maximum speed of the conveyor belt. If it is possible to keep the glue at the application temperature with a chip embedded for an extended time with out affecting the reliability of the system, then we will be able to quickly deploy a chip and place the components correspondingly closer together. To adjust for varying conveyor velocities, we can either couple the timing of the applicator to the speed readout from the conveyor or place suitable tags on the conveyor belt itself at close intervals and have them read (and matched) by both the ABIS system and the applicator. To ensure that the MicroTAG chip actually hits the baggage item, we may have to adjust the lateral position or aiming direction of the applicator; the position of the item can be deduced from its x-ray image.

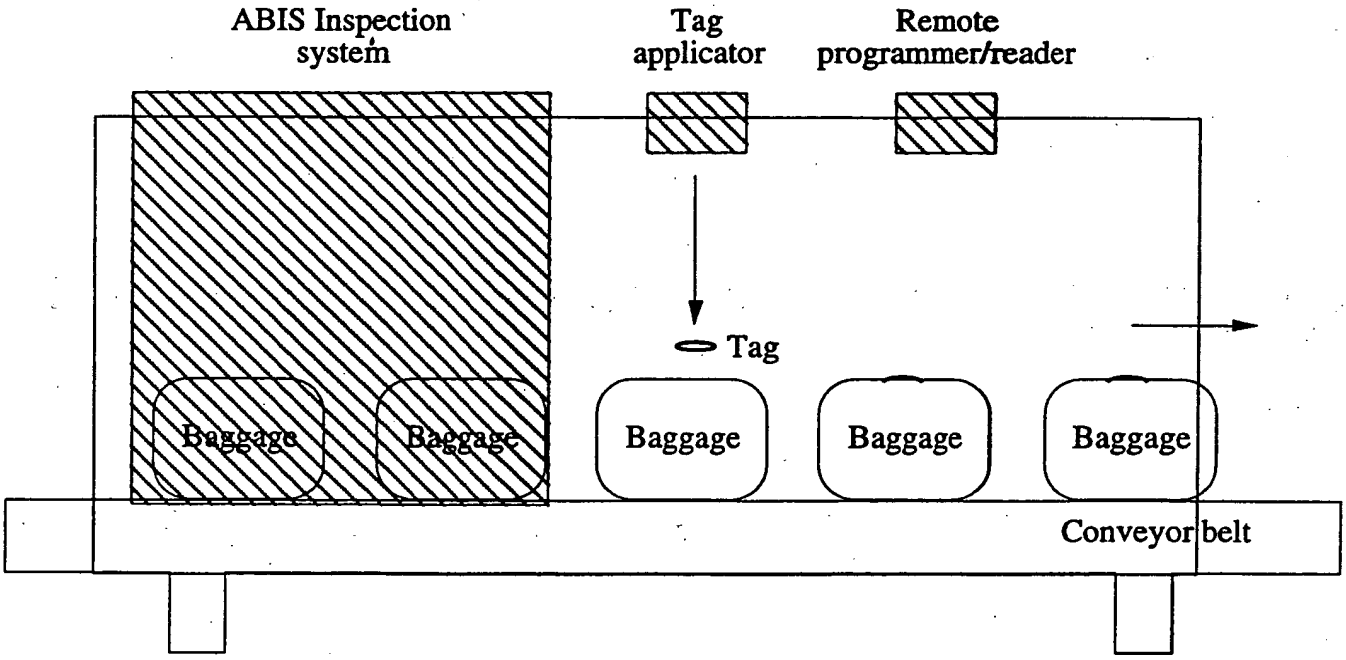

Figure 22: Schematic drawing of the integrated baggage inspection and tagging system. Sizes and distances are not to scale.

Immediately after it has been applied, the MicroTAG chip can be programmed and/or its ID number read by the remote programmer/reader and linked in the system's computer with the result of the inspection by the ABIS system. This also serves to verify that the chip has actually landed on the baggage as intended. Obviously, any preparation time for the programmer/reader will be much less than that for the applicator, so the two can be placed right next to one another.

D. 7 References

Ramo, S., J.R. Whinnery and T. Van Duzer, "Fields and Waves in Communication Electronics" Published by John Wiley and Sons, 1965.

E RELATED WORK

NOVA is developing state-of-the-art mixed signal multi channel ASIC chips for room temperature position sensitive solid state detectors such as silicon and CdZnTe strip, pixel, and pad arrays. These detectors with their readout electronics are developed to replace scintillator counterparts for application to industrial and medical imaging.

Six projects are presently under development at *NOVA*. The industrial projects are now in either Phase II or Phase III stages where engineering prototypes are being built or commercialized. The first project, Compact Integrated Narcotic Detection Instrument (CINDI) developed for *DoT/Coast Guard* has already started Phase III and being marketed and sold by our Phase III sponsor. This shows that *NOVA* is striving to carry out research and development with the sole aim of bringing state of the art products into commercial market.

The second project is a space based gamma ray detector for the detection and discrimination of nuclear warheads from decoys deployed by intercontinental ballistic missiles developed for *DoD/BMDO*. This project gave rise to a mixed signal (analog and digital) ASIC front-end readout (RENA) chip with 32 channels. It is developed to read out the new silicon strip and CdZnTe pad detectors. This chip has been designed to be versatile and flexible. It can be applied to most solid state detectors such as silicon, germanium, HgI_2 and CdZnTe strip or pad detectors without modification. This chip is now in Phase III commercialization phase. An improved commercial version is being fabricated. RENA product will be launched and actively marketed this Fall.

The third project is a nondestructive imaging inspection system for large and dense objects using x-rays. Both projects use silicon strip detectors. A derivative of the third project is also started. It is an Automatic Baggage Inspection System (ABIS) for *ARDEC, USDA* and *FAA*, a linear pixel CdZnTe pad detector array with 1 mm pitch (active area 4 mm x 32 mm) and a 32 channel fast mixed signal ASIC Front-end Electronics for Spectroscopy Application (FESA) chip for reading out these detectors are being developed. The first and second prototypes have been fabricated. The ceramic carrier, electronics, and test station have been made. The experience gained on the development of the FESA chip will be important for this project.

There are three major medical projects progressing at *NOVA*. The first project is the high sensitivity single photon emission computed tomography (SPECT) system. The second medical project is a scintimammography system for detecting and determine malignant breast cancer tumors. The third project is a high contrast digital mammography system. Two of these projects have been funded by *NIH* and the scintimammography project is funded by *DoD/Army*. Solid state detectors such as silicon strip, CdZnTe pad, and silicon pixel detectors are used in these projects. The design of a prototype pixel detector with its dedicated readout ASIC chip has been developed and tested. This is a charge integration type mixed signal ASIC chip with TDI capability different than the other ASIC chips. The second, full scale, version of this chip has been designed, manufactured, and functionally tested. This new front-end readout chip will bring new capability to *NOVA*'s solid state detectors. The experience gained on this third ASIC chip will be also important for the proposed project.

One more proposal, a CdZnTe pixel detector based high contrast digital mammography system is also awarded but the funding has not started yet. All these projects are based on solid sate detectors with custom mixed signal ASIC readout chips.

F RELATIONSHIP WITH FUTURE R&D WORK

F. 1 Anticipated Results of Phase II

The result of the Phase II work will be the development of a working smart MicroTAG system with remote controller and applicator that is ready for commercialization. The MicroTAG chip will be

manufactured, most likely, on silicon and will be completely self-contained, not requiring any external antennas or batteries. It will have small size and will be programmed and read out by a remote controller within a distance of ≥ 1 m. A MicroTAG applicator will be also developed that will place the MicroTAG chip on the scanned baggage or any item inside a tiny non-hardening glue ball which can be removed without affecting the surface of the item it is attached to.

F. 2 Significance of Phase II Results for Phase III Work

During Phase III the completed MicroTAG system will be designed into and manufactured as a commercial product and supplied to government and commercial sectors for field testing. It is intended to use the system initially for tagging suspicious baggage items in connection with the Automateic Baggage Inspection System under development at *NOVA* and *ARDEC*. Therefore, the proposed integration with *NOVA*'s ABIS system during the final stage of Phase II will provide us with valuable experience to successfully solve the problems to be expected in Phase III. Phases II and III are estimated to take about two years and one year each to complete, respectively.

G POTENTIAL FOLLOW-ON APPLICATIONS

G. 1 Commercial Application

Potential commercial application of a smart versatile tag is self evident and extremely good. It can be applied to monitoring, tracking, searching, labeling, personalizing, selecting, and finding items that belong to a large group. Due to the low production cost, the proposed radio frequency smart tags can be used to tag a large number of items without need to recover them. They can also be used in smart card type systems where access to the card can be done remotely. Potential civilian uses of the smart tags include: tagging luggage, bags, boxes in airports; monitoring parcels, packages, crates, and individual items during transport; identifying employees and vehicles; labeling and searching folders, files, and dockets; personalizing and recording information on smart cards; tracking inventory; and monitoring merchandise. Of course, some of these applications will require modifications to the system, such as using different ways to apply the chips and developing hand-held programmers/readers. These modifications are minor, though, and in view of the large potential market for the associated applications, they should be well worth the additional development effort.

The first deployment is expected to be in airports where there is a major need for smart tags by *USDA, FAA,* and the *US Customs.* The use by air transport companies for *FAA* and *USDA* alone can reach millions of tags per year. When all the other sectors are put together the ultimate use of the smart tags may approach a billion tags per year costing only few cents each in such large quantities.

The smart MicroTAG chip is straightforward to manufacture once the working design is completed. It will be fabricated in the form of large quantities of wafers in commercial chip foundries. They can be diced immediately since expensive wafer probing to select good chips will not be necessary. At this stage *NOVA* can take over the dies and pass them through an automatic conveyor-belt type test and selection system. The bad tags will be diverted and the good ones will be coated for protection and stored for shipment. Such a setup does not need major equipment and funding, and a small high-tech company like *NOVA* has the means to carry out this setup with reasonable venture capital funding. The potential of the smart MicroTAG chip is so well defined that once the technology is demonstrated finding venture capital is not expected to be difficult.

The development of the remote programmer/reader and the applicator provides a complete solution to the user. Although these will be shipped in smaller quantities compared to the smart MicroTAG chips they are also expected to bring major income to *NOVA*.

G. 2 Federal Government Use

The proposed radio frequency or microwave smart tags and applicator can be used for military and other government applications too. These applications will be quite similar to the applications listed

above. For example, some possible military applications include tagging individual weapons, munitions, pieces of equipment, crates, and other inventory. The government sector is expected to be an important customer for the smart MicroTAG chips and also the complete system with applicator.

H KEY PERSONNEL

H. 1 General

The key personnel include Dr. Jianping Peng (PI), Dr. Tümay O. Tümer (Co-PI), Dr. Martin Clajus (Co-I), Mr. Dale Maeding (Consultant), and Mr. Rene Brown (Consultant). They are all engineers with both chip development and mechanical design experience.

Dr. Jianping Peng (PI) is an engineer at *NOVA R&D, Inc.* A detailed resume of Dr. Peng can be found in section H. 2. In section H. 3 we list a selection of his recent publications.

Principal Investigator Dr. Jianping Peng is an engineer at *NOVA R&D, Inc.* He is in charge of the Automated Baggage Inspection System (ABIS) project development and plays a key role in this project: designing, testing, and debugging the FESA (Front-end Electronics for Spectroscopy Application) chips, testing the CdZnTe semiconductor detectors, and producing images of baggage on a conveyor belt by mounting the assembly of FESA chips and the CdZnTe detectors into an x-ray scanner. He has an excellent knowledge of electronics and experience in making electronic circuits and signal processors (both analog and digital). He also has the experience in overseeing the IC chip design. He is also developing the ABIS imaging software using C++.

Dr. Peng has a Ph.D. in physics from the *City University of New York*, and also a M.S. and B.S. in physics from the *Peking University* (P.R. China.). Before arriving at *NOVA* Dr. Peng was a research assistant at *Brookhaven National Laboratory.* His work consisted of research were he performed analysis of particle interaction with solids, particle annihilation, positron and electron scattering and channeling in single crystals. He also performed research involving ultra-high vacuum technology using mechanical, turbo-molecular, ion, and titanium sublimation pumps. In addition he worked with low temperature technology using a cryo-pump, cryostat, and cold head. He has also developed the electronics for these projects. He will carry out most of the tasks listed in the work schedule with the Co-PI and Co-I.

Vice-president Dr. T.O. Tümer is the Co-Principal Investigator for this project. He will be responsible to *NOVA* for the successful conclusion of this project. He has 30 years experience in detector design, development, and fabrication. Dr. Tümer has worked at *NOVA* since it was founded 13 years ago. He has over 75 publications in scientific journals and books and many more reports, presentations, and abstracts. He has supervised students and directed many research projects. He has extensive experience in fast electronics, ASIC chip development, gamma-ray and particle detectors, Compton double scatter techniques, and real-time data analysis. He has also extensive experience in silicon and CdZnTe strip, pad, and pixel detectors and their applications. He is the PI of two Phase II contracts, one for *DoD/BMDO* for a space-borne gamma-ray detector for gamma rays from 0.3 to 30 MeV and the other for *DoD/Army* on nondestructive inspection of munition items with x-rays. He is also the PI of two recently awarded projects on medical imaging, scintimammography and digital mammography. He will oversee the development and commercialization of the proposed smart MicroTAG system.

Dr. Martin Clajus has a Ph.D. in physics from *ETH* Zürich (Switzerland) and a M.S. (Diplom) in physics from the University of Bonn (Germany). Prior to joining *NOVA*, Dr. Clajus was a postgraduate research associate at the *University of California, Los Angeles.* During this time, as well as in the course of his dissertation, he has participated in experiments in intermediate energy particle and nuclear physics at various international accelerator facilities, most recently at *Brookhaven National Laboratory.* The focus of the research in which he has been involved was eta-meson physics, studying the properties of this particle and using it as a probe for baryon spectroscopy and to

investigate charge-symmetry breaking. Dr. Clajus has extensive experience using various types of radiation detectors such as semiconductor detectors, organic and inorganic scintillators, wire chambers, and gas Cherenkov counters. This experience includes the setup and adjustment of the associated trigger and readout electronics. Starting at the end of 1993, he was the primary responsible person for setting up and maintaining the front-end electronics for all experiments in which his group at UCLA has participated. His second major responsibility during this period was the development of a simulation program for a large solid angle photon calorimeter consisting of nearly 700 NaI crystals. He has authored or coauthored ten scientific papers and given oral presentations at international conferences and workshops. Since coming to *NOVA*, Dr. Clajus has mostly worked on Phase I of the smart MicroTAG project discussed in this proposal. He will be the main engineer assigned to this project.

Mr. Dale Maeding has had over 25 years of professional experience, first with *Hughes Aircraft Company*, then with *Silicon Systems Inc.*, and in the past ten years as an independent consultant. At *Hughes*, he was involved in the early developments of infrared focal plane array imaging devices in the Electrooptic Division. Later he designed integrated CCD signal processing devices at *Hughes Newport Beach Research Center*. In 1976 he became Section Head of Circuit Design at the *Hughes Carlsbad Research Center*. There he designed the readout electronics for several monolithic and hybrid Infrared Focal Plane Arrays as well as CCD signal processing devices.

For *Silicon Systems* he designed custom mixed signal ASICs with a specialization in analog design. He designed a wide variety of products from read/write amplifiers and servo controllers for disk drive products to modems, phonetic speech synthesizers, adaptive delta modulators, and tone decoders. He managed a standard cell development group, where analog approaches to CAD design were formulated.

In 1987 he set up a consulting practice for integrated circuit design. He has continued designing analog integrated circuits in bipolar, CMOS, and BiCMOS during this period of time. Some of the circuits include ethernet LAN transceiver, IRDA receiver, OTA video filter set, high speed A/D converters, and others. He has extensive experience in low noise integrated circuit design in the government and industrial sectors. Mr. Maeding has a B.S. degree in electrical engineering from Colorado State University and an M.S. degree, also in electrical engineering, from *UCLA*.

Presently Mr. Maeding is working with *NOVA R&D, Inc.* for the development of mixed signal integrated circuits for x-ray, gamma-ray, and particle detectors. He has already completed the Readout Electronics for Nuclear Application (RENA) chip layout and is now working on the digital mammography (MARY) chip. He will consult on the simulation and silicon layout of the smart MicroTAG ASIC chip.

Mr. Rene Brown founded *Lasair Design* and is the principal engineer and owner. Mr. Brown has 20 years of experience, 16 of which have been with *Hughes Aircraft Company*. He has designed circuits in silicon, germanium, and GaAs. He has designed 15 focal plane arrays for various applications. Mr. Brown has been involved in many high speed design projects at *Hughes*. Previous designs include high-speed ECL logic operating at 200 MHz, complementary JFET logic capable of 80 ps propagation delays, low noise 3 GHz bandwidth low power amplifiers for CO_2 laser systems, a fiber optic receiver using a GaAs transimpedance amplifier and high speed CMOS logic (100 MHz) for infrared CCD imagers, HgCdTe and InSb detectors hybridized to CCD and CMOS readouts, germanium readouts using JFET circuits for amplifiers and logic, GaAs readout with a capacitive transimpedance amplifier using MESFET devices, and BICMOS readouts with differential or folded cascode preamplifiers. He has designed many digital logic circuits including designs in SOS, CMOS, ECL, and IIL logic. He has also investigated logic designed in ferroelectric, GaAs MESFETs, and germanium JFETs. He has designed analog integrated circuits for radiation hard requirements and has extensive test experience with circuits in cryogenic, gamma, and x-ray environments. Mr. Brown has MS and BS degrees in electrical engineering from the *University of California at Davis*. He has authored or coauthored seven papers on focal plane arrays and signal processing for focal

plane arrays. Mr. Brown is a registered Professional Engineer in the *State of California* (E 11255). He will consult on the remote programmer/reader system for the smart MicroTAG ASIC chip.

All members of the key personnel plan to take part in Phase II of this project, are entirely committed and are determined to make the proposed project a great success.

H. 2 Resume of the Principal Investigator

JIANPING PENG: *NOVA R&D, Inc.*

Education:	Peking University (P.R. China)	B.S.	1984	Physics
	Peking University	M.S.	1987	Physics
	City University of New York (USA)	Ph.D.	1996	Physics

Professional Experience:

9/89 to 1/92	Teaching Assistantship and Research Assistantship: Dept. of Physics, City University of New York.
2/92 to 12/95	Research Assistantship: Dept. of Physics and Materials Science Division, Brookhaven National Laboratory.
1/96 to Present	Engineer, *NOVA R&D, Inc.*

H. 3 Related Publications from the Past Three Years

1. Vacancy defects in photoexcited GaAs studied by positron two-dimensional angular correlation of annihilation radiation, J.P. Peng, K.G. Lynn, M.T. Umlor, D.J. Keeble, and D.R. Harshamm, Phys. Rev. B **50** (Rapid communication), 11247 (1994).
2. Observation of diffraction effects in positron channeling, J.C. Palanthingal, J.P. Peng, K.G. Lynn, X.Y. Wu, and P.J. Schultz. In: Proceedings of the 10th International Conference on Positron Annihilation, p. 193 (1994).
3. Quantum channeling effects for 1 MeV Positrons, R. Haakensasen, L. Hau, J.C. Chelovchenko, J.C. Palachingal, J.P. Peng, P. Asoka-Kumar, K.G. Lynn, Phys. Rev. Lett **75** 1650 (1995).
4. Study of the Silicon-Dioxide/silicon interface using variable energy positron two-dimensional angular correlation of annihilation radiation, J.P. Peng, K.G. Lynn, P. Asoka-Kumar, D.P. Becker, D.R. Harshman, Phys. Rev. Lett. **76**, 2157 (1996).
5. Defects identification using core-electron contributions in Doppler broadening spectroscopy of positron annihilation, S. Szpala et al., Phys Rev. B **54**, 4722 (1996).
6. On the role of classical and quantum notions in channeling and the development of fast positron as a solid state probe of valence and spin density, L. Hau et al., Nucl. Instr. Methods B **119**, 30 (1996).
7. Preliminary Results from a Novel CdZnTe Linear Pad Detector Array X-ray Imaging System, Jianping Peng, Tümay O. Tümer, Brian Petrini, Scott Kravis and Shi Yin, SPIE Proc. **2859**, 319 (1996).

I FACILITIES AND RESOURCES

Laboratory: The ASIC chip development and testing electronics and detector development laboratory at *NOVA R&D, Inc.* will be available for this work. The facilities also include state of the art test

equipment for wafer probing and wire bonding capability, calibration and evaluation of radiation detectors.

Computer: *NOVA R&D, Inc.* has many computers available for the simulation and optimization of the detectors. Software development for chip tests and for the remote programmer/reader can also be carried out. The computers include Unix workstations and top performance IBM-compatible and Macintosh desktop computers.

Office: The offices at *NOVA R&D, Inc.* will be available for this project. The offices include excellent report and paper generation capabilities and an experienced purchasing department.

Major Equipment: *NOVA R&D, Inc.* has the following equipment available for this project: a Pantak HF-160 x-ray system that generates x-ray photons up to 160 keV; nine computers; a logic analyzer, an ultrasonic wire bonder, a wafer probe station, a spectrum analyzer; three oscilloscopes; a multichannel analyzer; a CAMAC crate with controller; an NIM crate; many NIM modules (spectroscopy amplifier, single channel analyzer with pulse shape discrimination capability, discriminator, ratemeter, a versatile 4 channel logic module, fan-in/out unit, dual channel counter/timer, time to amplitude converter, precision pulse generator with detector pulse output simulation capability); high and low voltage power supplies; GAL and EPROM programmers; electronic measurement devices; high resolution multimeter; printed circuit manufacture system; a Class 10000 cleanroom; environmental chambers with temperature and humidity control capability; and many homemade special detector test electronics and boards. All the equipment will be available for the proposed research without charge.

Additional information: *NOVA R&D, Inc.* has been involved in developing sophisticated electronics devices, mixed signal ASIC chips, and radioactivity detectors since 1984. The company has a sophisticated electronics laboratory and a small machine shop. *NOVA* has laboratory space available for this project and a radiation licence to use radioactive sources and x-ray generators in its research. There are many gamma ray, electron, and positron sources available which could be used in the proposed development project. *NOVA* facilities meet environmental, federal, and California state laws and regulations. It has management and support services to supplement the laboratory work. *NOVA* is currently developing several products . The expertise gained in these projects is expected to help the proposed smart MicroTAG system development significantly and expedite its successful completion.

Innovative Design: Innovative Design has excellent facilities. The computers used for silicon layout are fully capable of schematic capture, circuit simulation, and logic simulation. The computers also have design software for layout, schematic capture, DRC (design rule check), and LVS (logic verification of layout versus schematic). The current processors are set up for advanced computer aided design. The tape outputs are the industry standard GDS-II for integrated circuits or converted for compatibility with Artwork Conversion software to other desirable formats. All the systems include full tape backup, large format monitors, modems, and high speed video cards. An E size continuous feed plotter interfaces to the design computers to create high resolution color plots to provide visual checking of our design work. Innovative Design is in compliance with all state, federal, and local environmental laws and regulations.

Lasair Design: Lasair Design has excellent facilities. Among many equipment the directly related facilities for this work are a prototype breadboard and fabrication work area which is equipped to build up a test printed circuit design as required for final check out of printed circuit designs. This area is also used to test integrated electronics and circuit boards. A computer controlled laser micro machining station provides precision work in cutting sapphire, GaAs, silicon, stainless steel, and other hard substances. Lasair Design is in compliance with all state, federal, and local environmental laws and regulations.

J CONSULTANTS

The main consultants for the MicroTAG chip design are Mr. Dale Maeding and Mr. Rene Brown. Their experience is discussed in the Key Personnel section.

K PRIOR, CURRENT AND PENDING SUPPORT

There is no prior, current or pending support received or expected to be received for the proposed work.

PROPRIETARY

APPENDIX C

U.S. DEPARTMENT OF DEFENSE
SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM

COST PROPOSAL

1. **NAME OF OFFEROR:** NOVA R & D, Inc.

2. **HOME OFFICE ADDRESS:** 1525 Third Street, Suite C, Riverside, CA 92507-3429
Telephone: (909) 781-7332, Fax: (909) 781-0178

3. **LOCATION WHERE WORK WILL BE PERFORMED:** Same as above

4. **TITLE OF PROPOSED EFFORT:**
Low Cost Practical MicroTAG and a Tag Applicator System

5. **TOPIC NUMBER AND TOPIC TITLE:**
A96-009, Low Cost Radio Frequency Smart Tags and Applicator

6. **TOTAL DOLLAR AMOUNT OF THE PROPOSAL:** $749,887

7. DIRECT MATERIAL COST:	Year 1	Year 2
a) Purchased parts		
General supplies (PCBs, electronic components, cables, etc.)	$15,000	$15,000
Tag chip foundry charge (MOSIS process)	20,000	68,000
Electronics circuits and parts for fabricating remote programmer/reader	30,000	20,000
Parts and supplies for manufacturing MicroTAG applicator	10,000	20,000
b) Subcontracted items		
MicroTAG chip silicon layout (Innovative Design)	60,000	20,000
Machine-shop work for MicroTAG applicator	10,000	10,000
d) Total direct material	145,000	153,000
9. DIRECT LABOR: (with 5% salary increase during the second year)		
Principal Investigator: Dr. Jianping Peng, 2,500 hr @ $24.26/hr	30,325	31,841
Co-Principal Investigator: Dr. Tümay Tümer, 200 hr @ $44.65/hr	4,465	4,688
Co-Investigator: Dr. Martin Clajus, 4,036 hr @ $22.50/hr	45,405	47,675
Test Engineer: Gerard Visser, 400 hr @ $20.10/hr	4,020	4,221
Engineer: Lan Doan, 200 hr @ $18.00/hr	1,800	1,890
Technician: Min Wei, 600 hr @ $14.00/hr	4,200	4,410
Total direct labor	90,215	94,725

10. LABOR OVERHEAD (G & A Included):		
100.2% (overhead rate) @ $90,215 and $94,725 (Base: direct labor)	90,395	94,914
13. TRAVEL:		
One week trip to ARDEC for two engineers to deliver and train operators		
Airfare for two engineers		1,600
Per diem for two engineers for one week @ $90 per day		1,260
Car rental @ $45 per day		315
Total Travel		3,175
14. CONSULTANTS:		
a) **Identification**		
Dale Maeding - MicroTAG chip design, simulation and silicon layout, ... hr @ $95 /hr	15,000	2,500
Rene Brown - MicroTAG chip testing, evaluation and interrogator design, ... hr @ $65 /hr	7,500	1,000
Total Consultant	**22,500**	**3,500**
TOTAL COST	**348,110**	**349,314**
18. FEE: 7.5% @ $348,255 and $349,314 (Total costs)	26,108	26,198
19. TOTAL ESTIMATED COST AND FEE: (Both years)		**$749,730**

20. TYPED NAME AND TITLE, SIGNATURE AND DATE OF SUBMISSION

Tümay O. Tümer, Vice-President  August 6, 1997

21. a) Has any executive agency of the United States government performed any review of your accounts or records in connection with any other government prime contract or subcontract within the past twelve months? **YES** (March 6, 1997, DCAA, Western Region, San Gabriel Valley Branch Office, West Covina, CA 91790-2900, Ph: (818) 918-5922.)

b) Will you require the use of any government property in the performance of this proposal? **NO**

c) Do you require government contract financing to perform this proposed contract? **YES (Progress Payments)**

22. TYPE OF CONTRACT PROPOSED: COST PLUS FIXED FEE

Tag Chip Photo:

000107